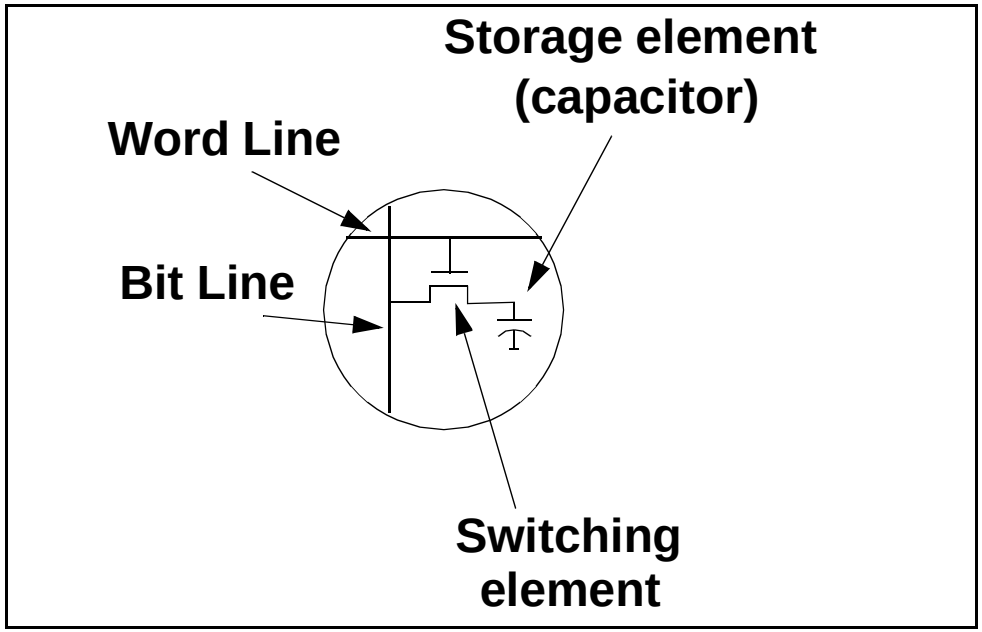
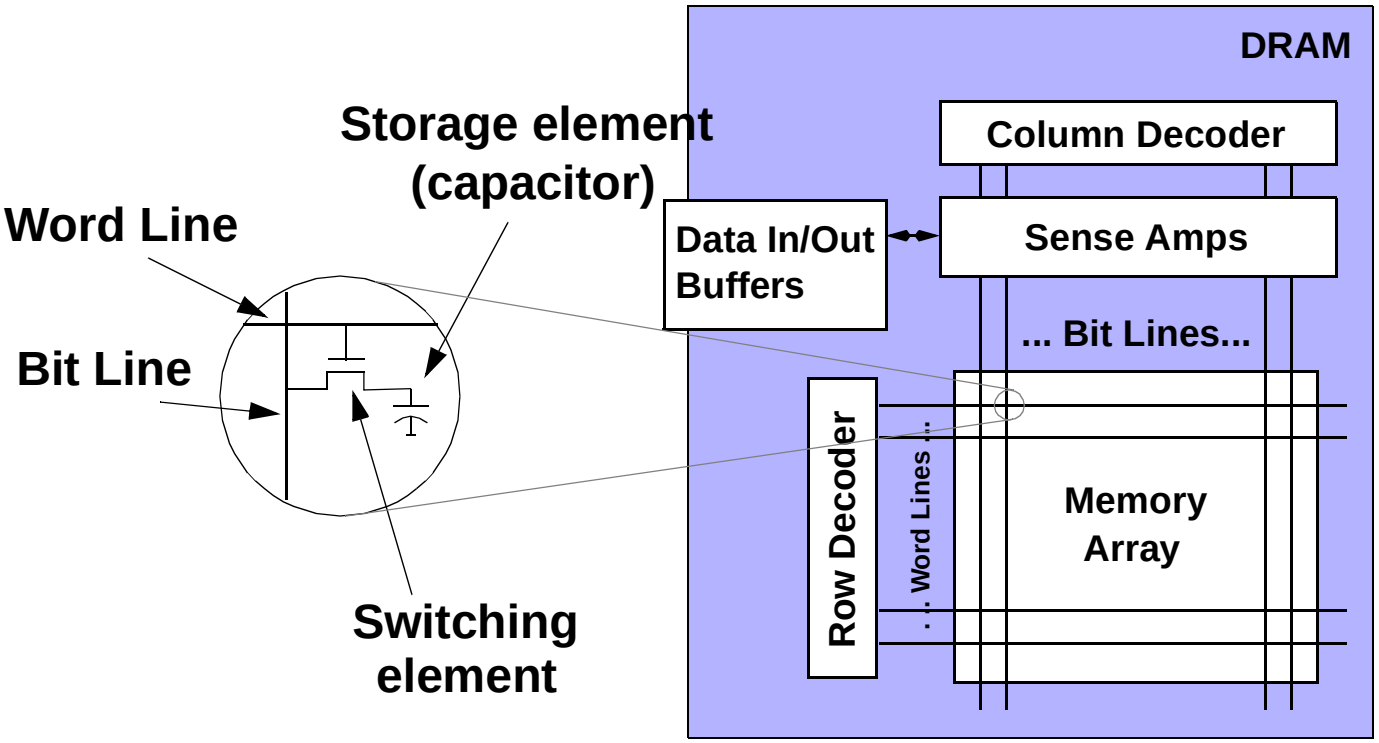
DRAM Circuit and Architecture Basics

- **Overview**
- **Terminology**
- **Access Protocol**
- **Architecture**



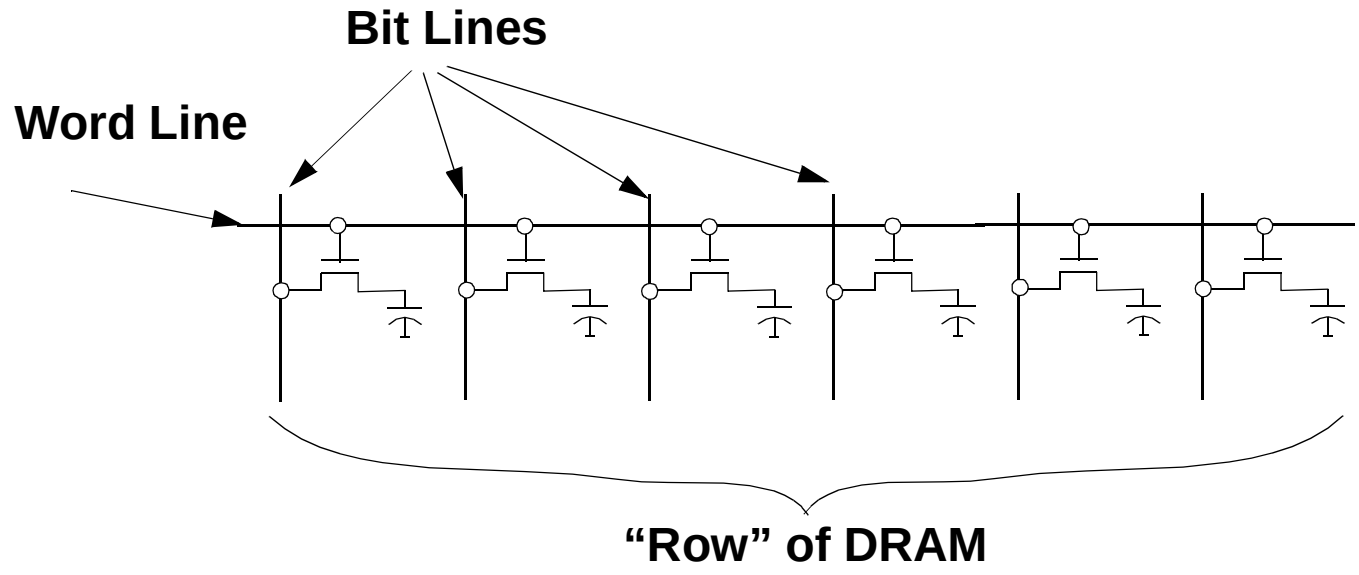
DRAM Circuit Basics

DRAM Cell



DRAM Circuit Basics

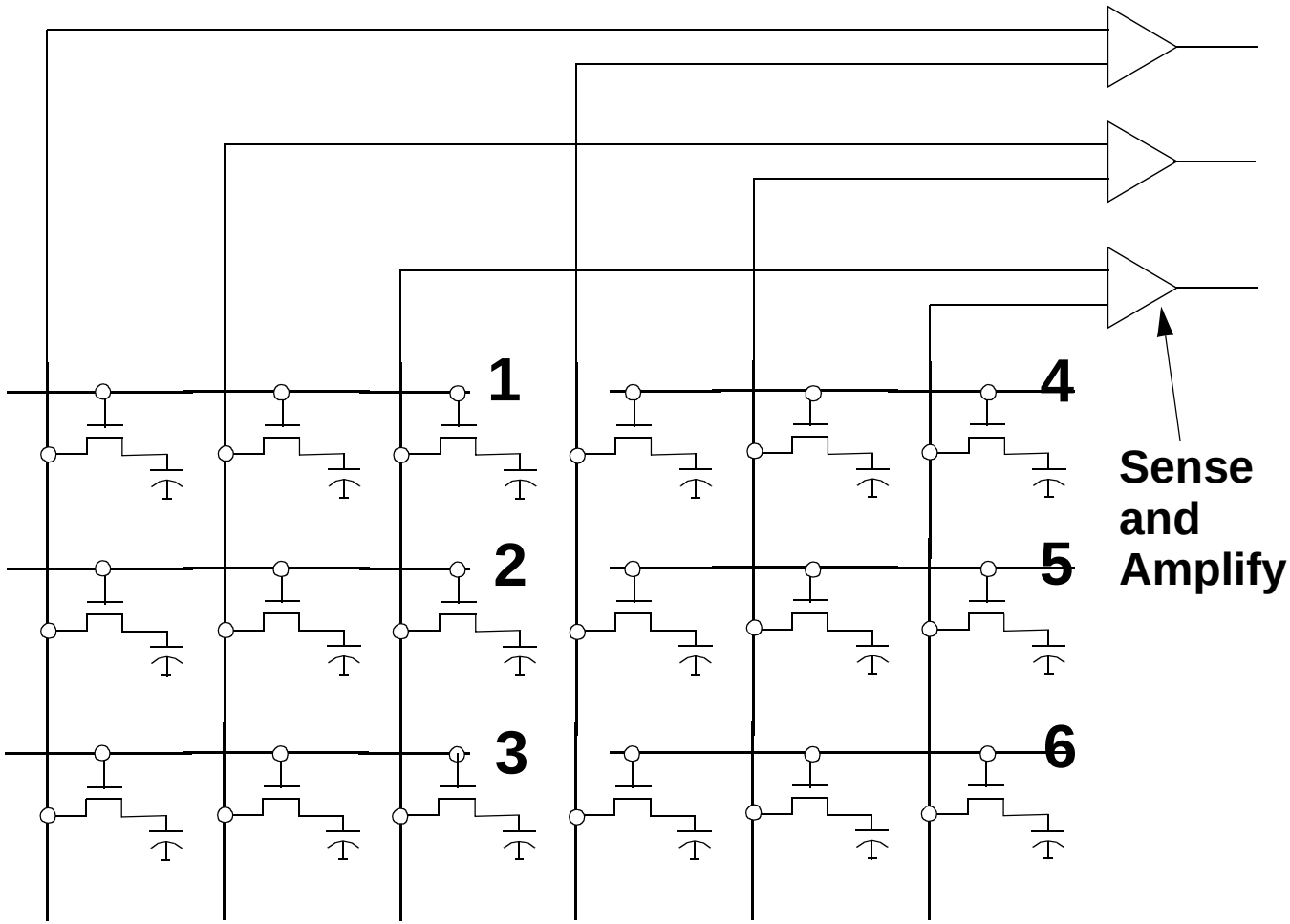
“Row” Defined



Row Size: 8 Kb @ 256 Mb SDRAM node
4 Kb @ 256 Mb RDRAM node

DRAM Circuit Basics

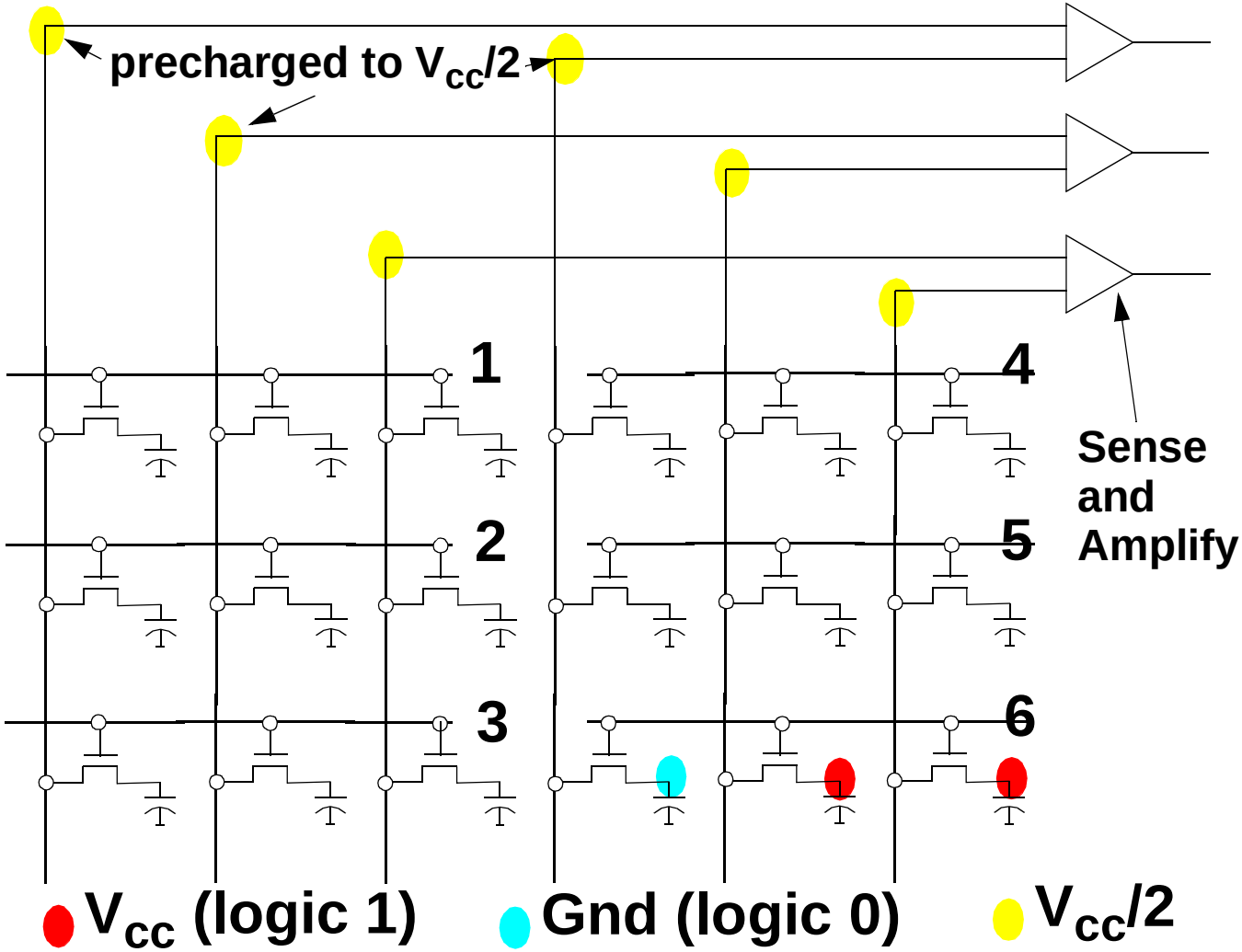
Sense Amplifier I



6 Rows shown

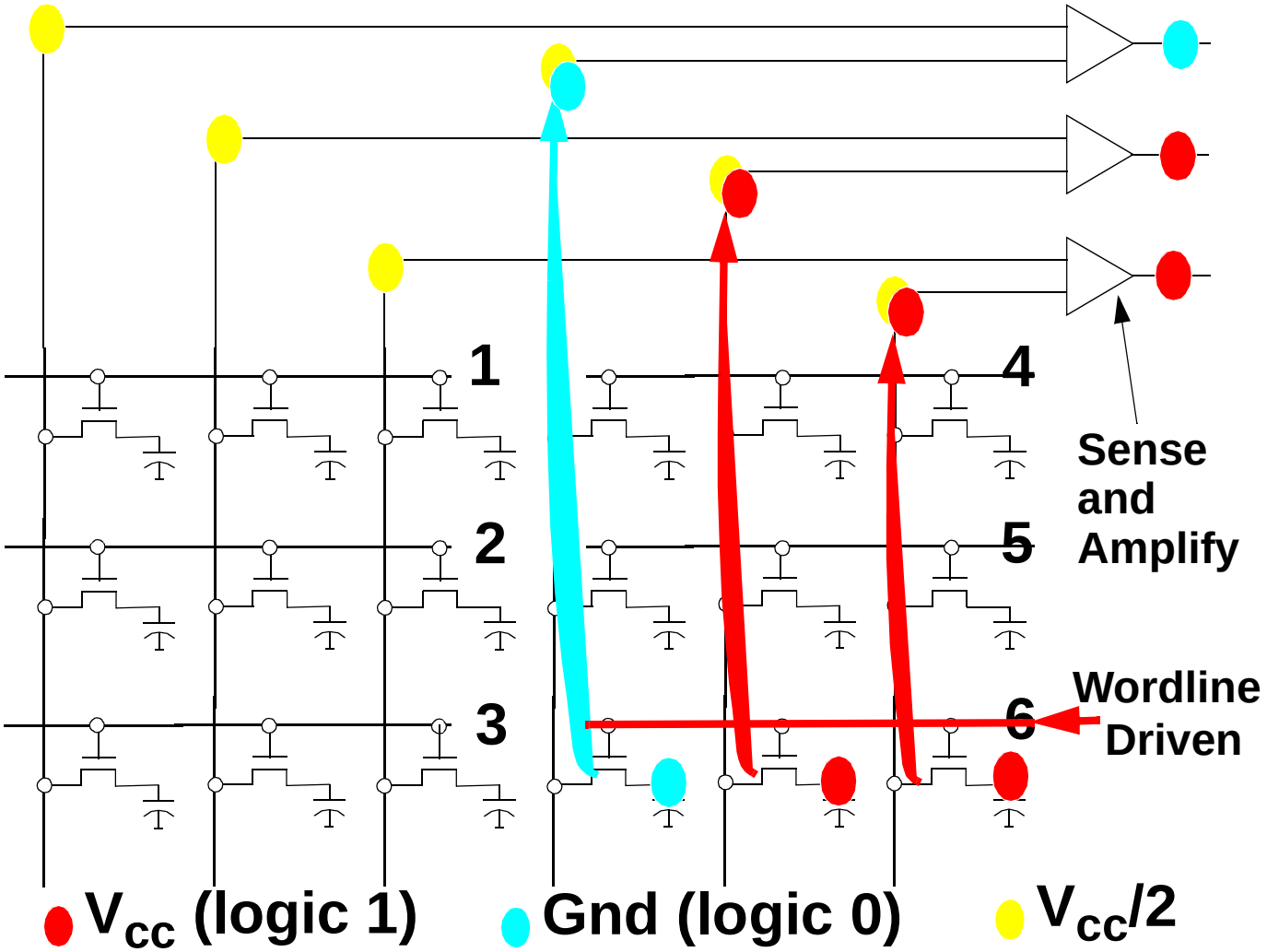
DRAM Circuit Basics

Sense Amplifier II : Precharged



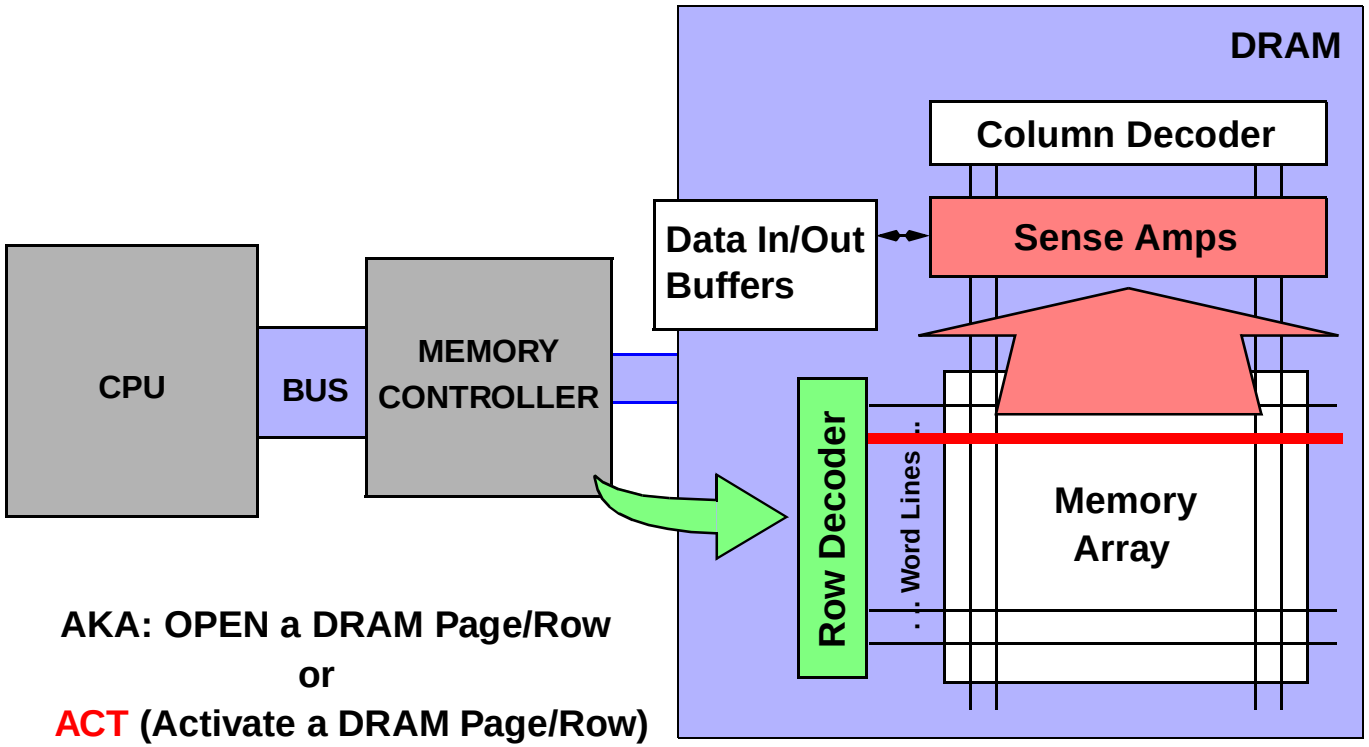
DRAM Circuit Basics

Sense Amplifier III : Destructive Read



DRAM Access Protocol

ROW ACCESS



AKA: OPEN a DRAM Page/Row
or
ACT (Activate a DRAM Page/Row)
or
RAS (Row Address Strobe)

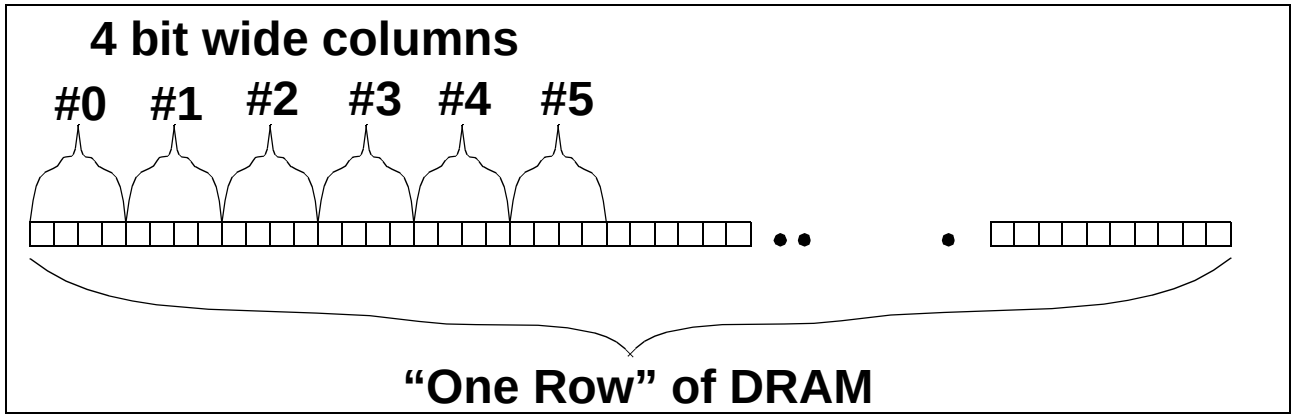
DRAM Circuit Basics

“Column” Defined

Column: Smallest addressable quantity of DRAM on chip

SDRAM*: column size == chip data bus width (4, 8,16, 32)
RDRAM: column size != chip data bus width (128 bit fixed)

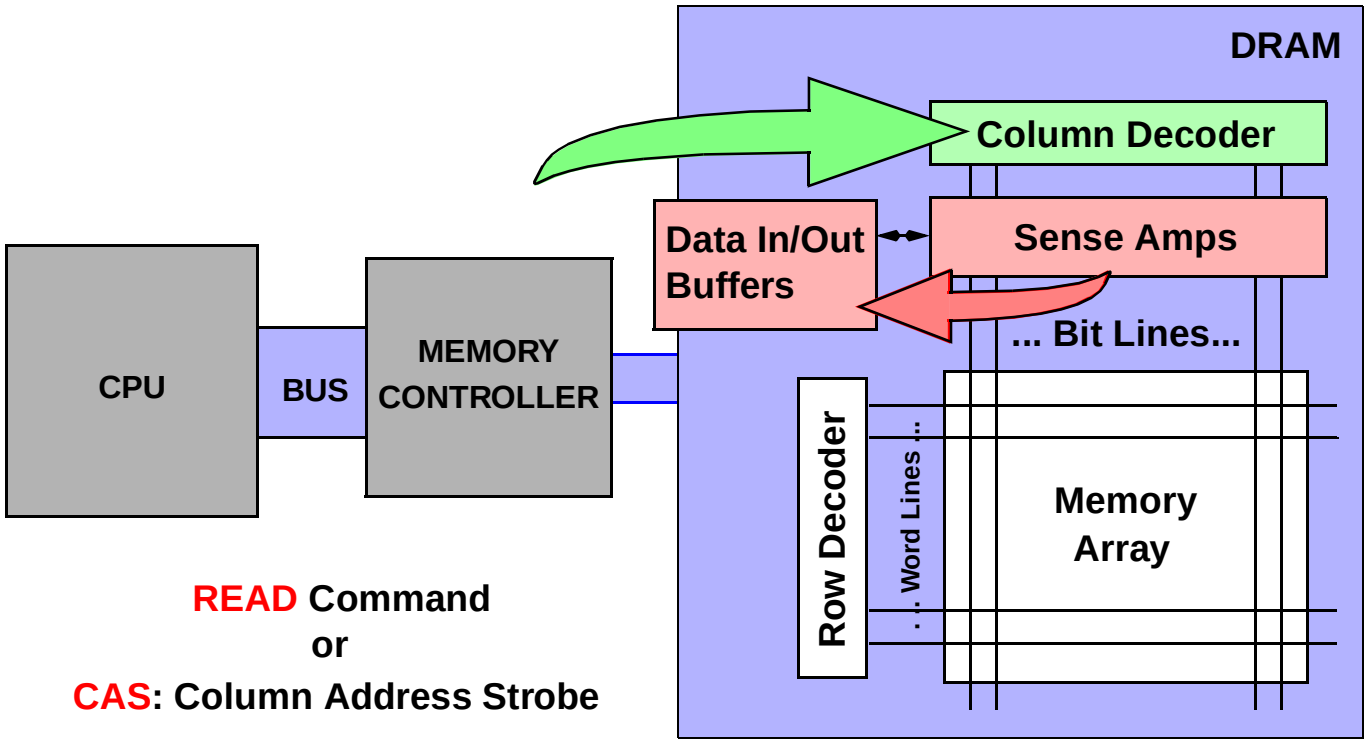
SDRAM*: get “n” columns per access. n = (1, 2, 4, 8)
RDRAM: get 1 column per access.



*** SDRAM means SDRAM and variants. i.e. DDR SDRAM**

DRAM Access Protocol

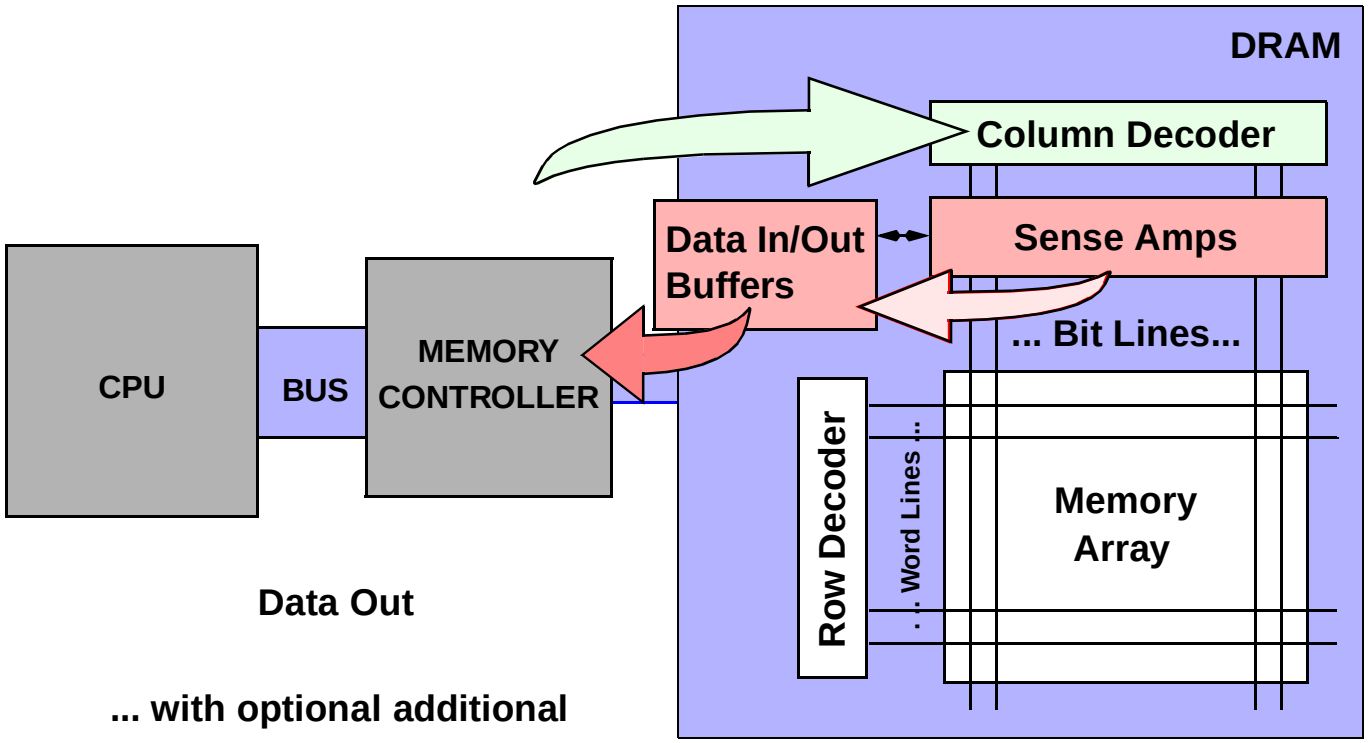
COLUMN ACCESS I



READ Command
or
CAS: Column Address Strobe

DRAM Access Protocol

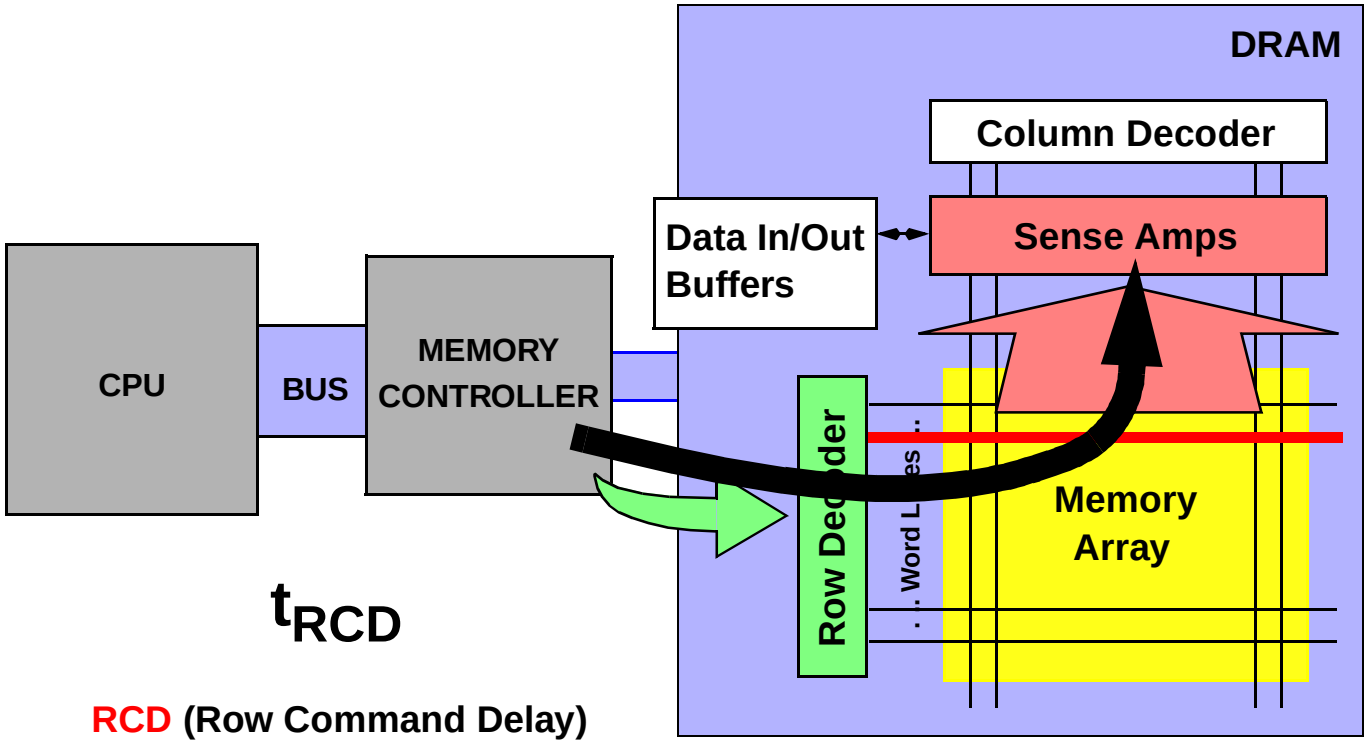
Column Access II



note: page mode enables overlap with CAS

DRAM "Speed" Part I

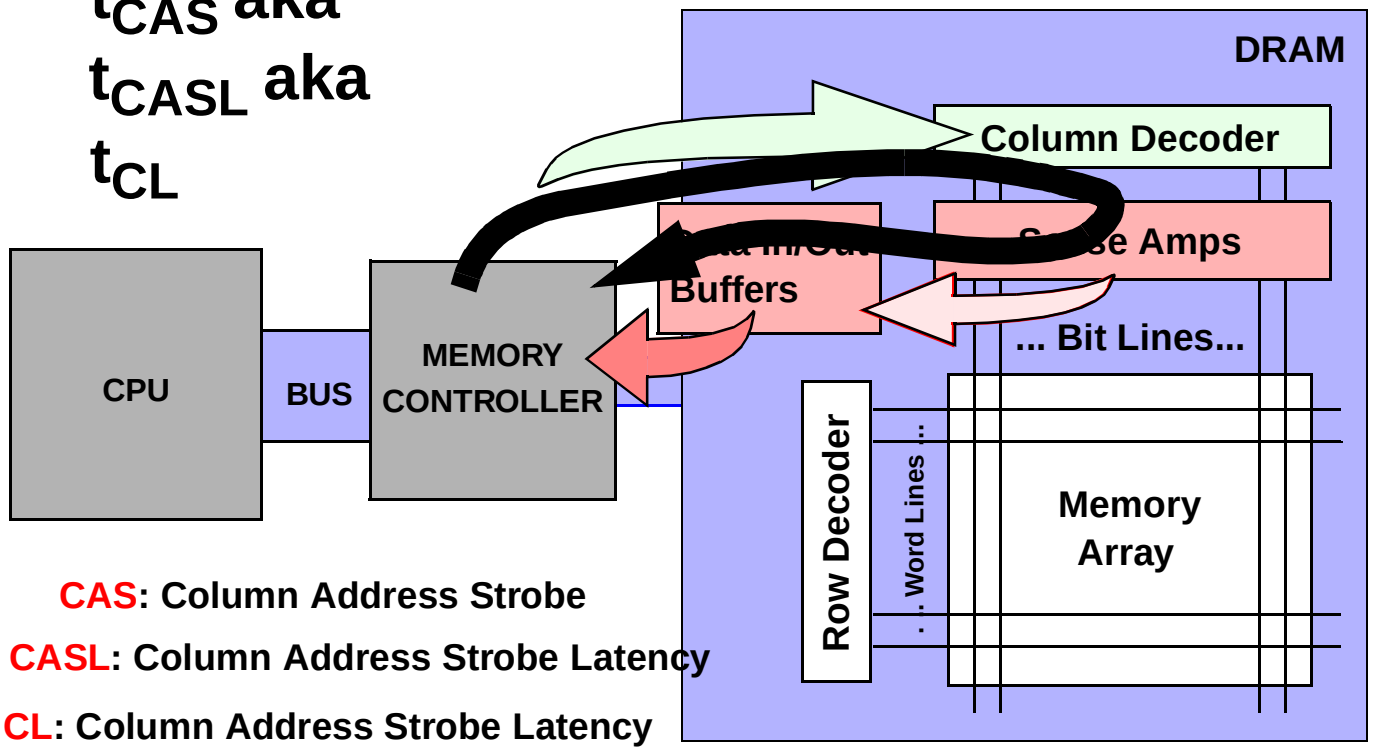
How fast can I move data from DRAM cell to sense amp?



DRAM "Speed" Part II

How fast can I get data out of sense amps back into memory controller?

t_{CAS} aka
t_{CASL} aka
t_{CL}



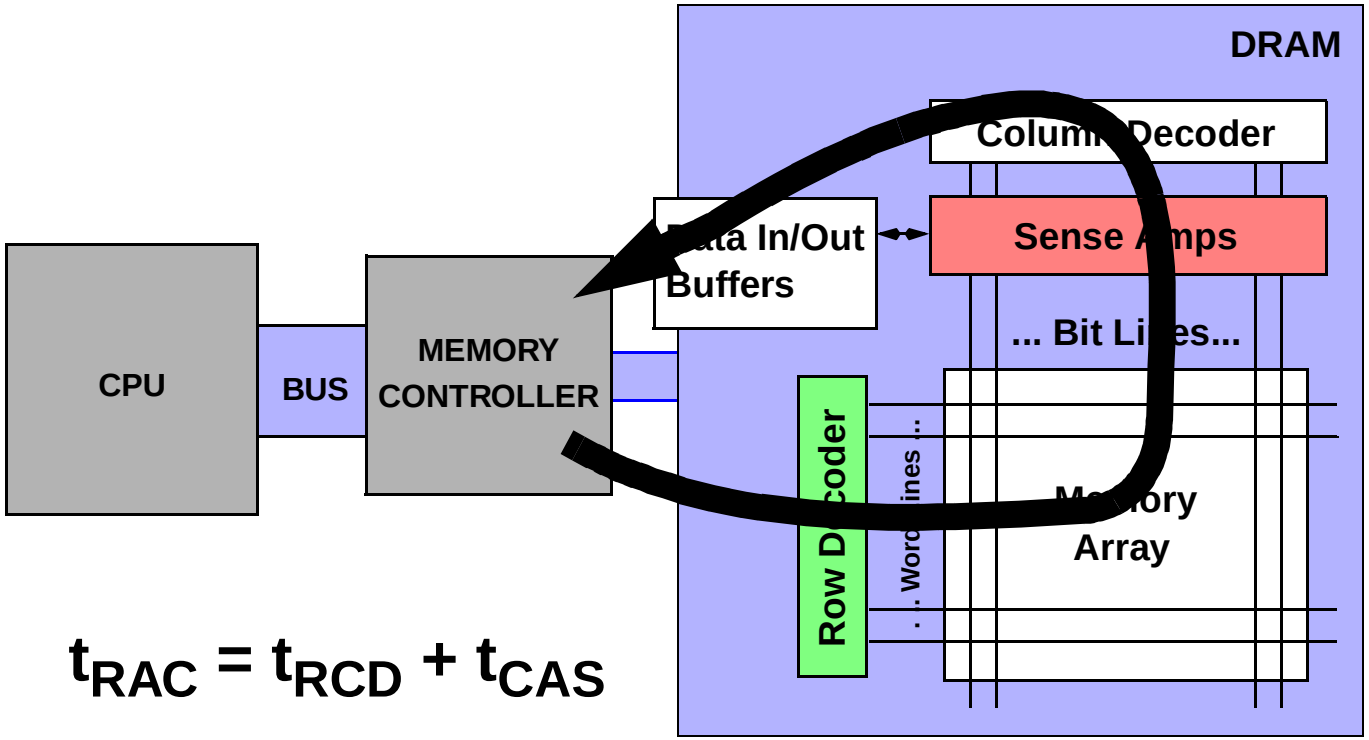
CAS: Column Address Strobe

CASL: Column Address Strobe Latency

CL: Column Address Strobe Latency

DRAM "Speed" Part III

How fast can I move data from DRAM cell into memory controller?

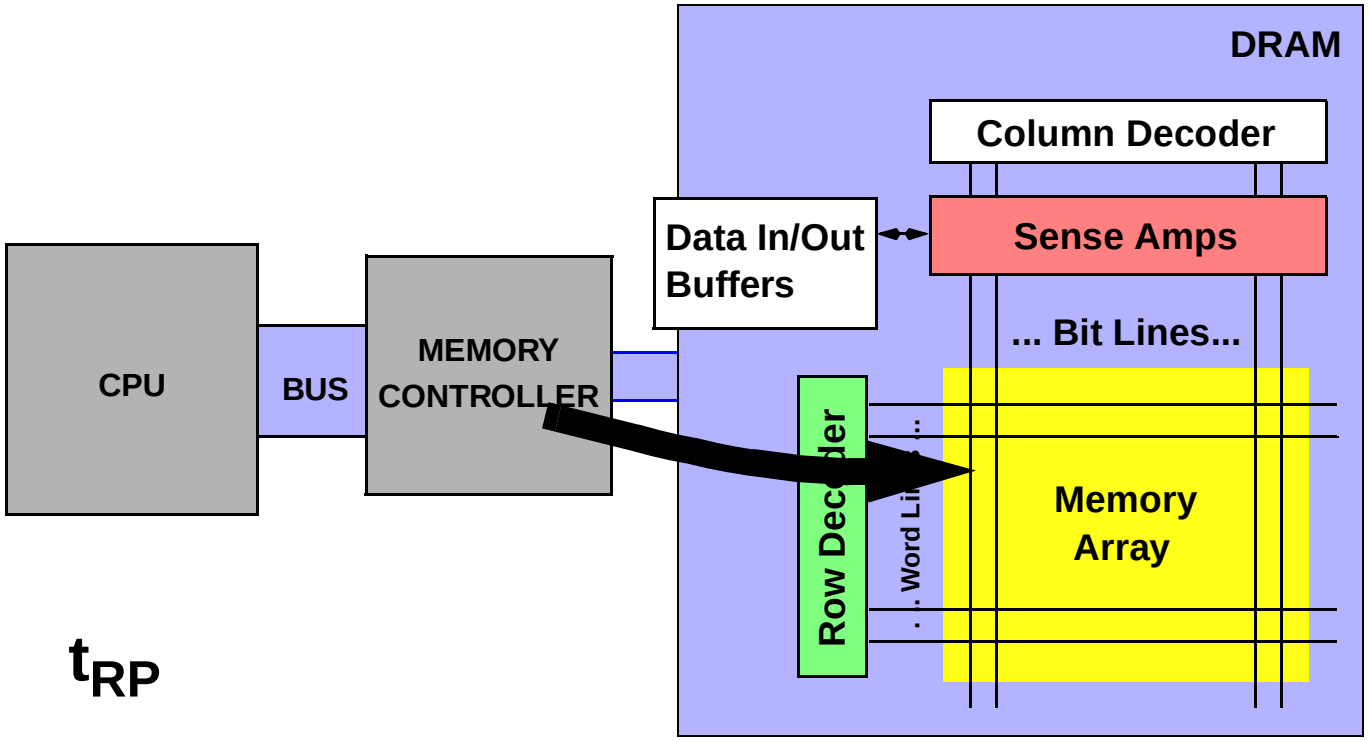


$$t_{RAC} = t_{RCD} + t_{CAS}$$

RAC (Random Access Delay)

DRAM "Speed" Part IV

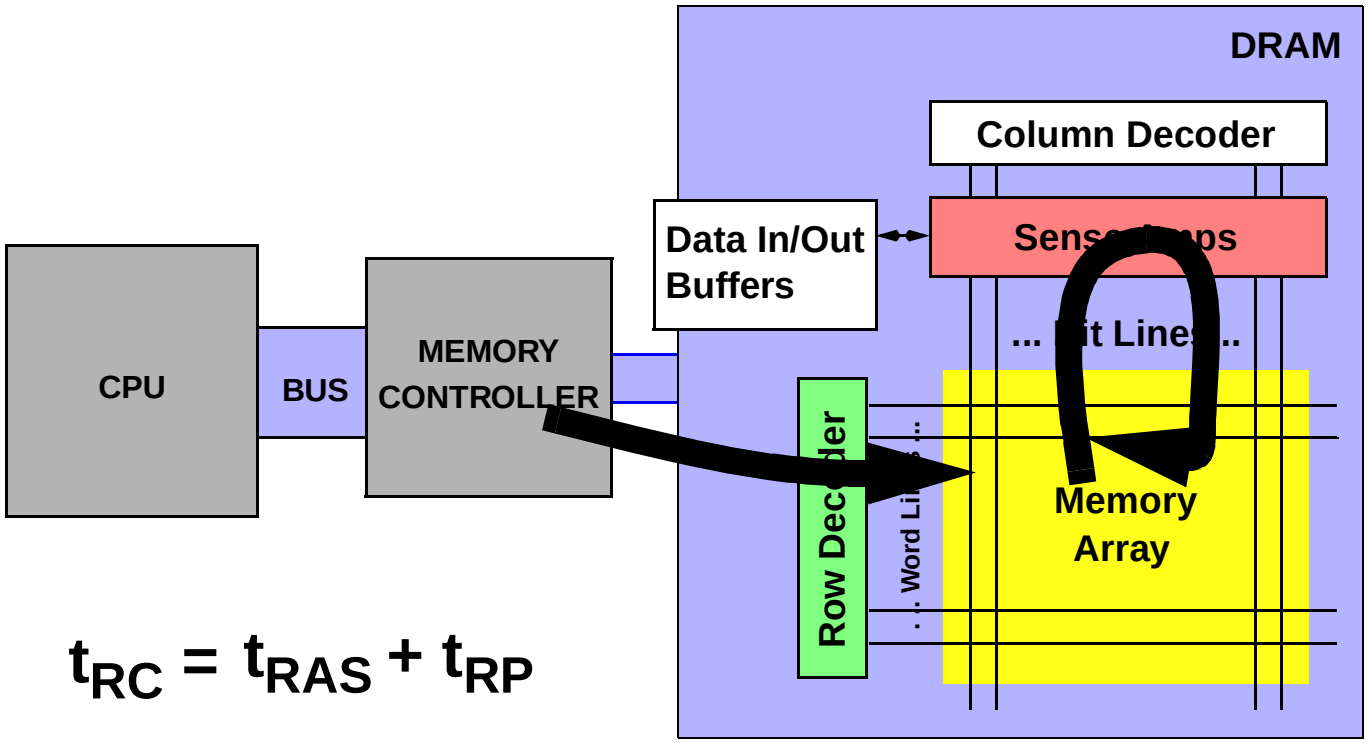
How fast can I precharge DRAM array so I can engage another RAS?



RP (Row Precharge Delay)

DRAM "Speed" Part V

How fast can I read from different rows?



$$t_{RC} = t_{RAS} + t_{RP}$$

RC (Row Cycle Time)

DRAM "Speed" Summary I

What do I care about?

t_{RCD}

t_{CAS} ← Seen in ads. Easy to explain Easy to sell

t_{RP}

$t_{RC} = t_{RAS} + t_{RP}$ ← Embedded systems designers DRAM manufactuers

$t_{RAC} = t_{RCD} + t_{CAS}$ ← Computer Architect: Latency bound code i.e. linked list traversal

RAS: Row Address Strobe

CAS: Column Address Strobe

RCD: Row Command Delay

RAC :Random Access Delay

RP :Row Precharge Delay

RC :Row Cycle Time

DRAM "Speed" Summary II

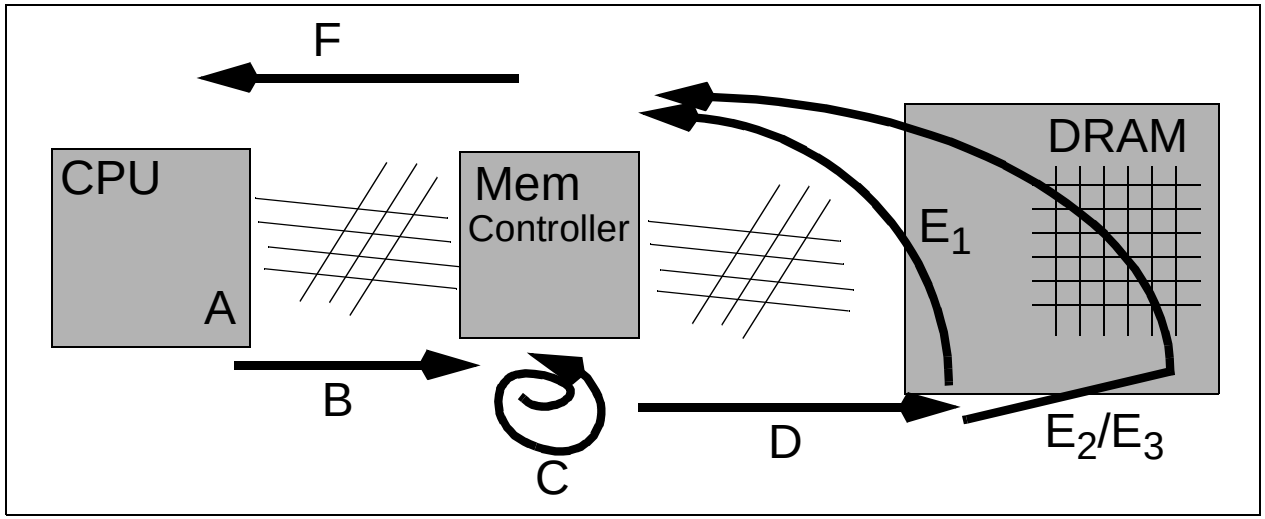
DRAM Type	Frequency	Data Bus Width (per chip)	Peak Data Bandwidth (per Chip)	Random Access Time (t_{RAC})	Row Cycle Time (t_{RC})
PC133 SDRAM	133	16	200 MB/s	45 ns	60 ns
DDR 266	133 * 2	16	532 MB/s	45 ns	60 ns
PC800 RDRAM	400 * 2	16	1.6 GB/s	60 ns	70 ns
FCRAM	200 * 2	16	0.8 GB/s	25 ns	25 ns
RLDRAM	300 * 2	32	2.4 GB/s	25 ns	25 ns

DRAM is "slow"
But doesn't have to be
t_{RC} < 10ns achievable

Higher die cost → Not adopted in standard

Not commodity → Expensive

"DRAM latency"

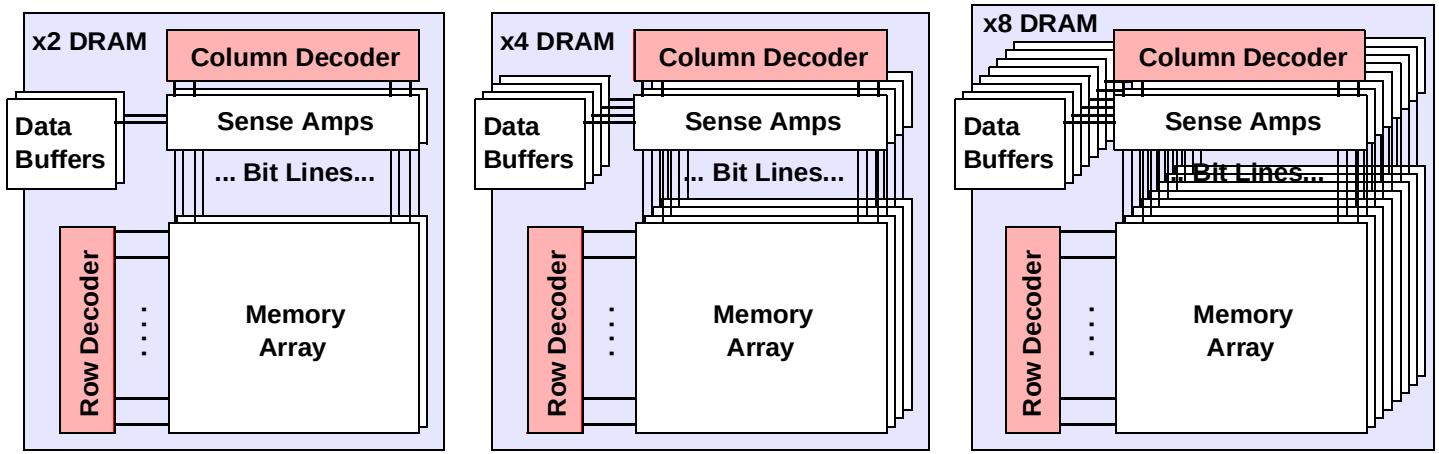


A: Transaction request may be delayed in Queue
B: Transaction request sent to Memory Controller
C: Transaction converted to Command Sequences (may be queued)
D: Command/s Sent to DRAM
E_1: Requires only a **CAS** or
E_2: Requires **RAS + CAS** or
E_3: Requires **PRE + RAS + CAS**
F: Transaction sent back to CPU

"DRAM Latency" = A + B + C + D + E + F

DRAM Architecture Basics

PHYSICAL ORGANIZATION



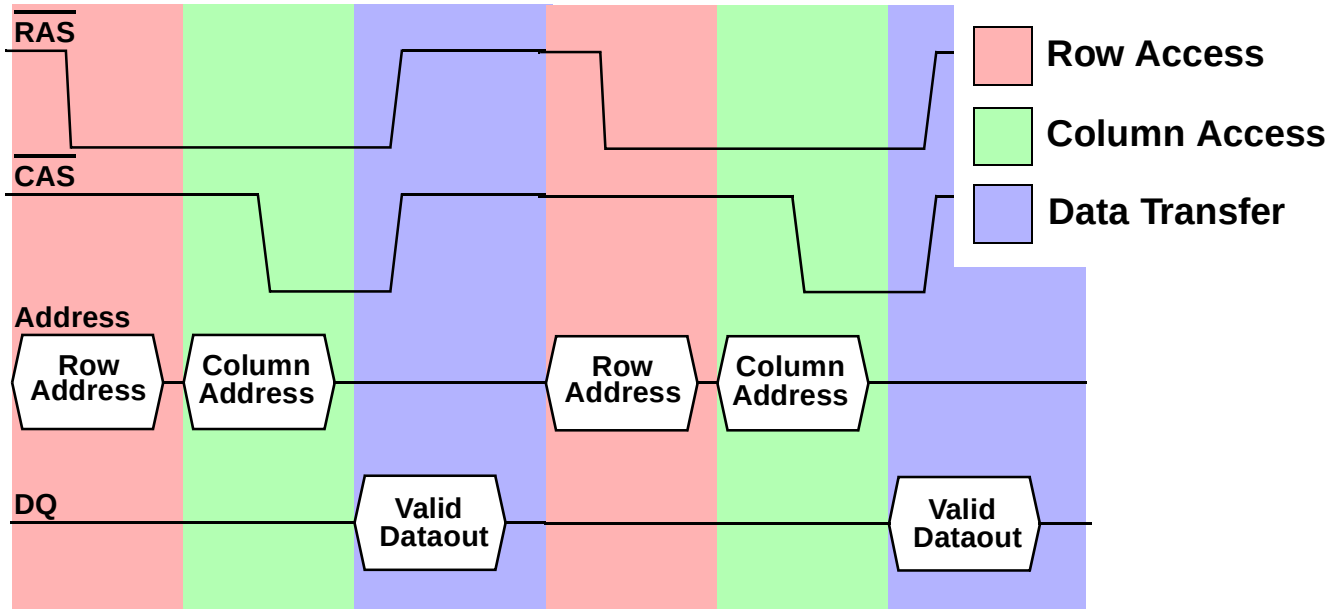
x2 DRAM **x4 DRAM** **x8 DRAM**

This is per bank …

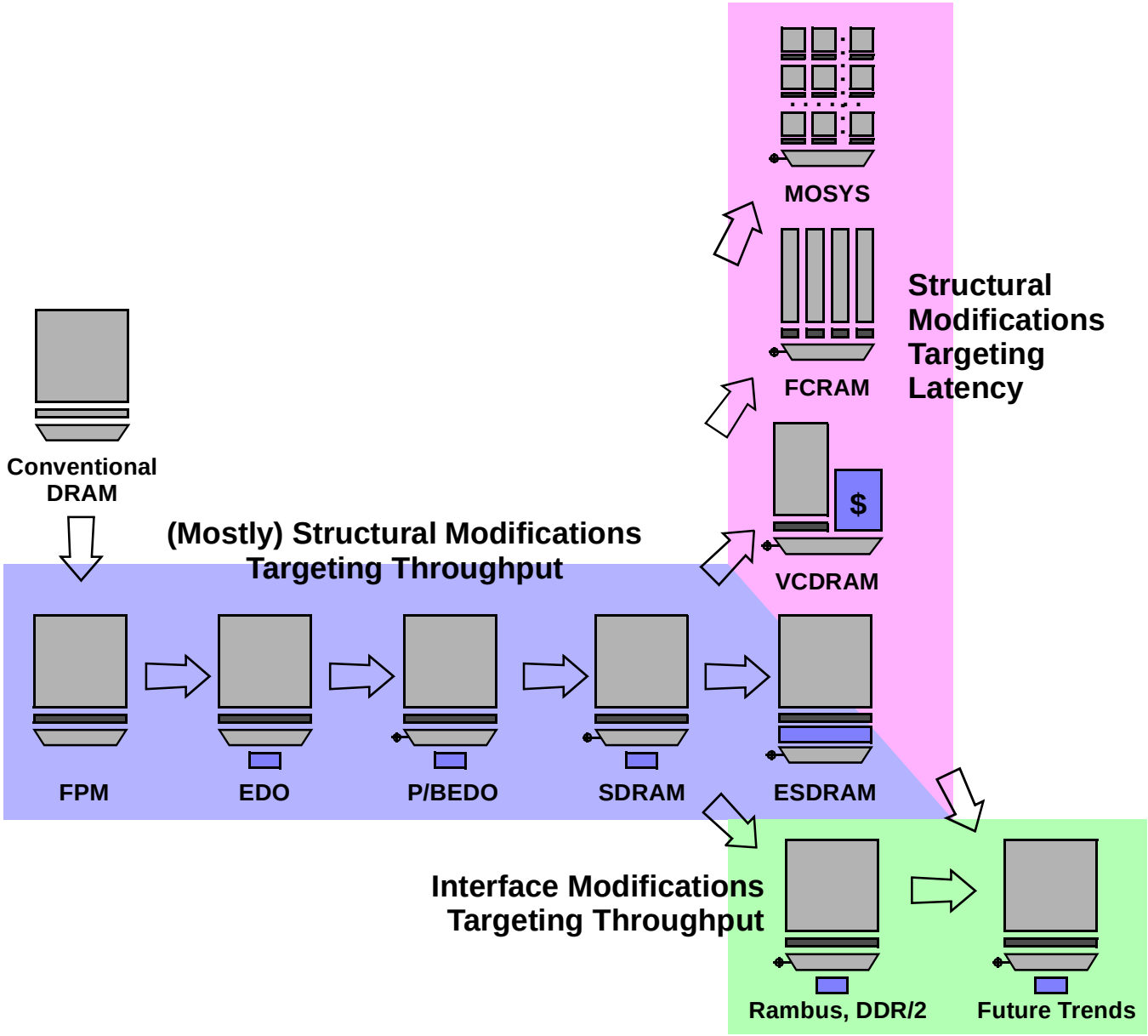
Typical DRAMs have 2+ banks

DRAM Architecture Basics

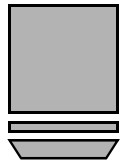
Read Timing for Conventional DRAM



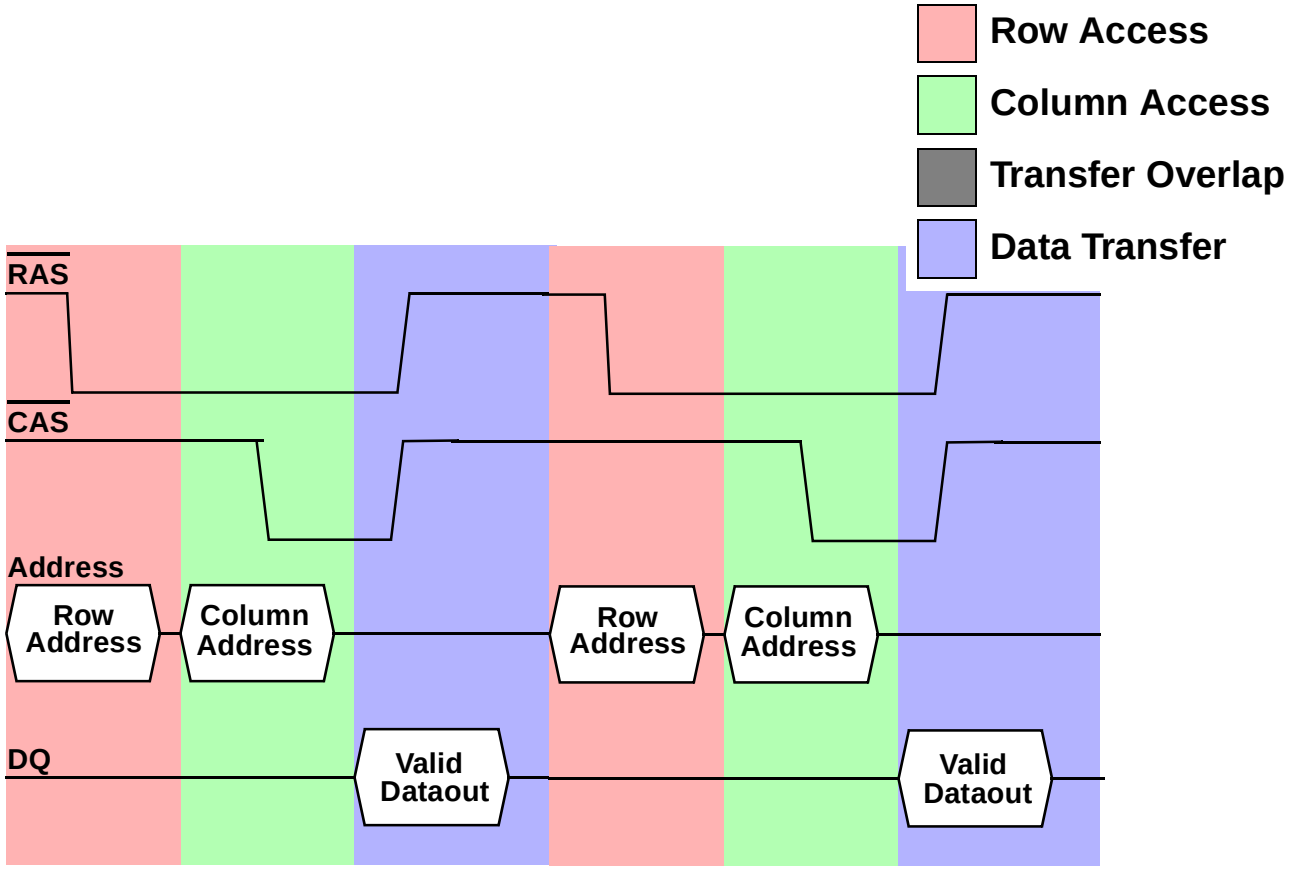
DRAM Evolutionary Tree



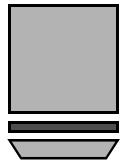
DRAM Evolution



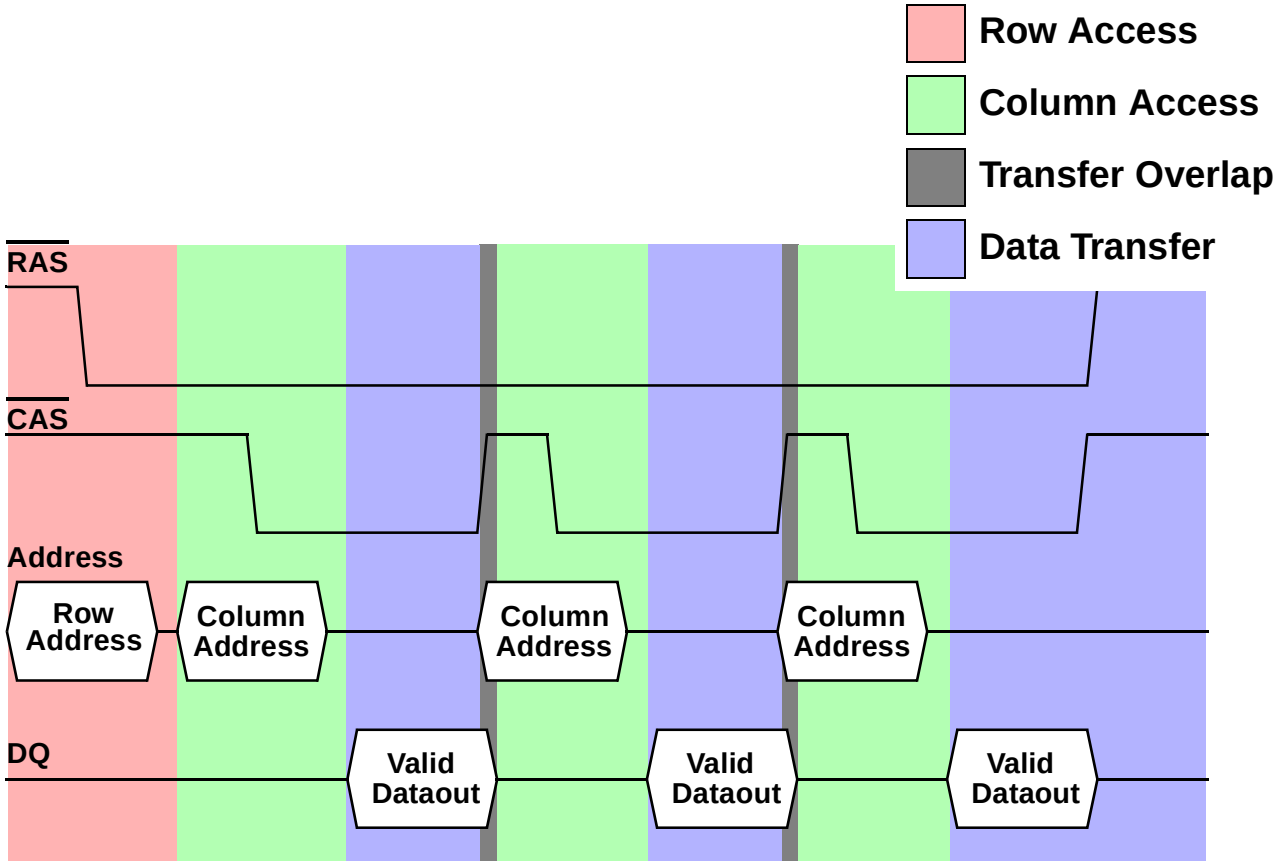
Read Timing for Conventional DRAM



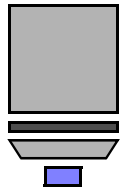
DRAM Evolution



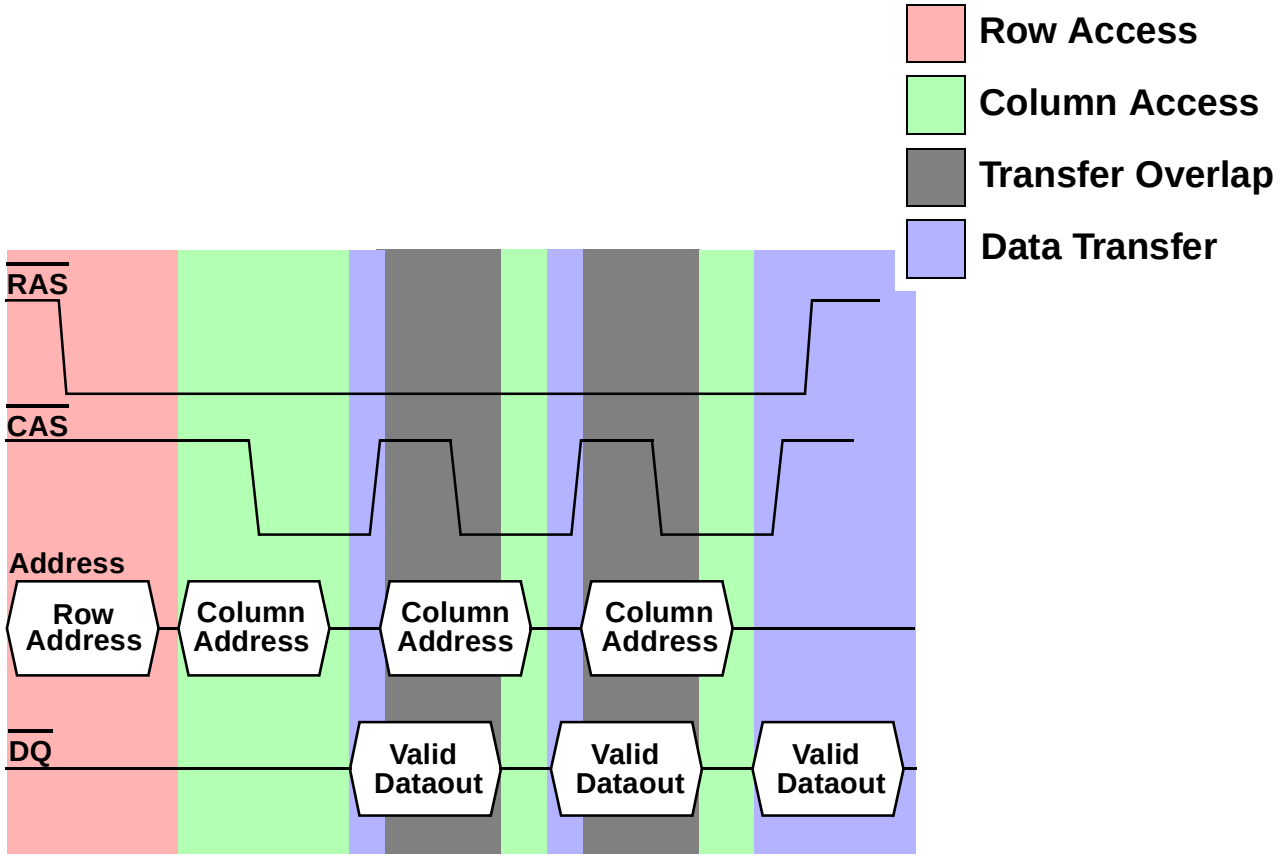
Read Timing for Fast Page Mode



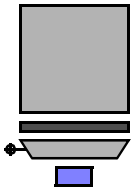
DRAM Evolution



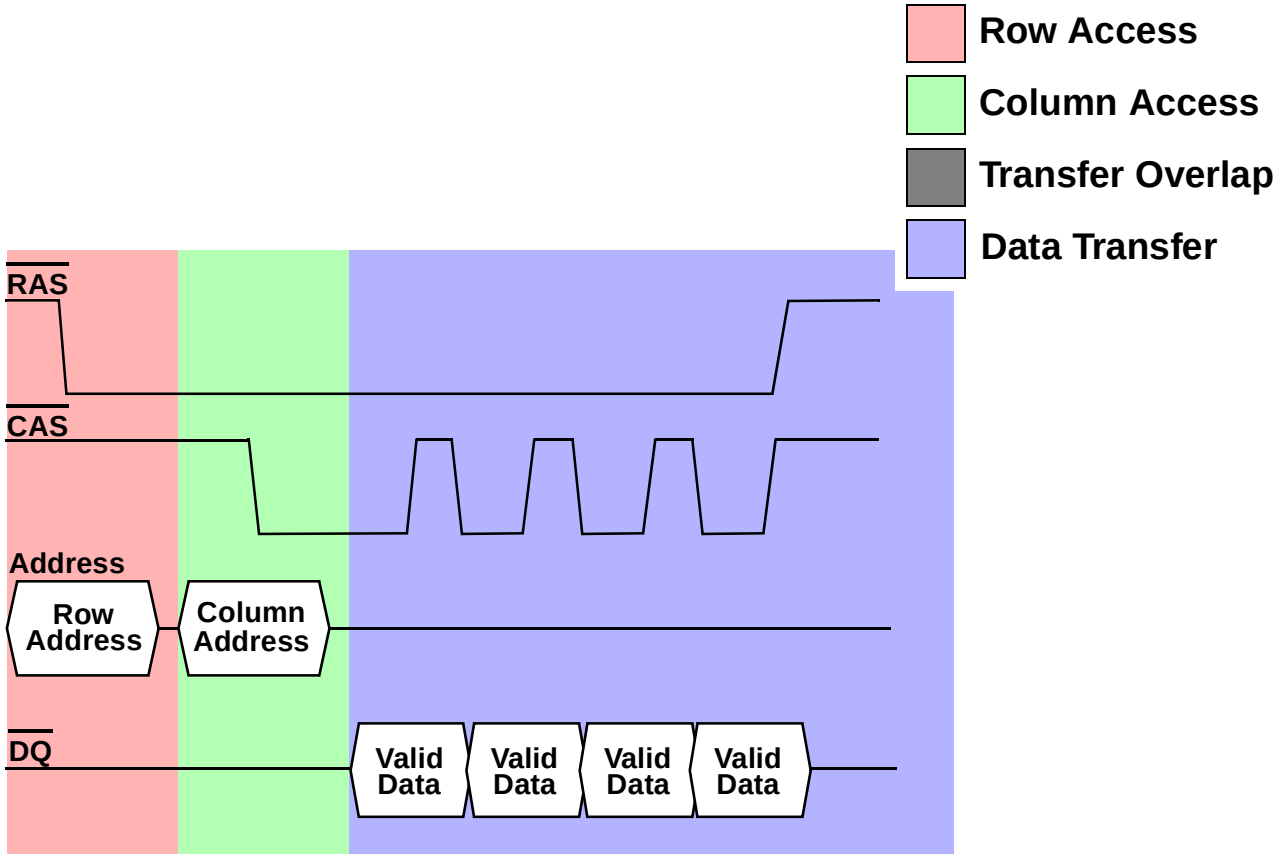
Read Timing for Extended Data Out



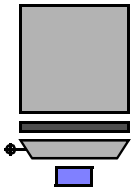
DRAM Evolution



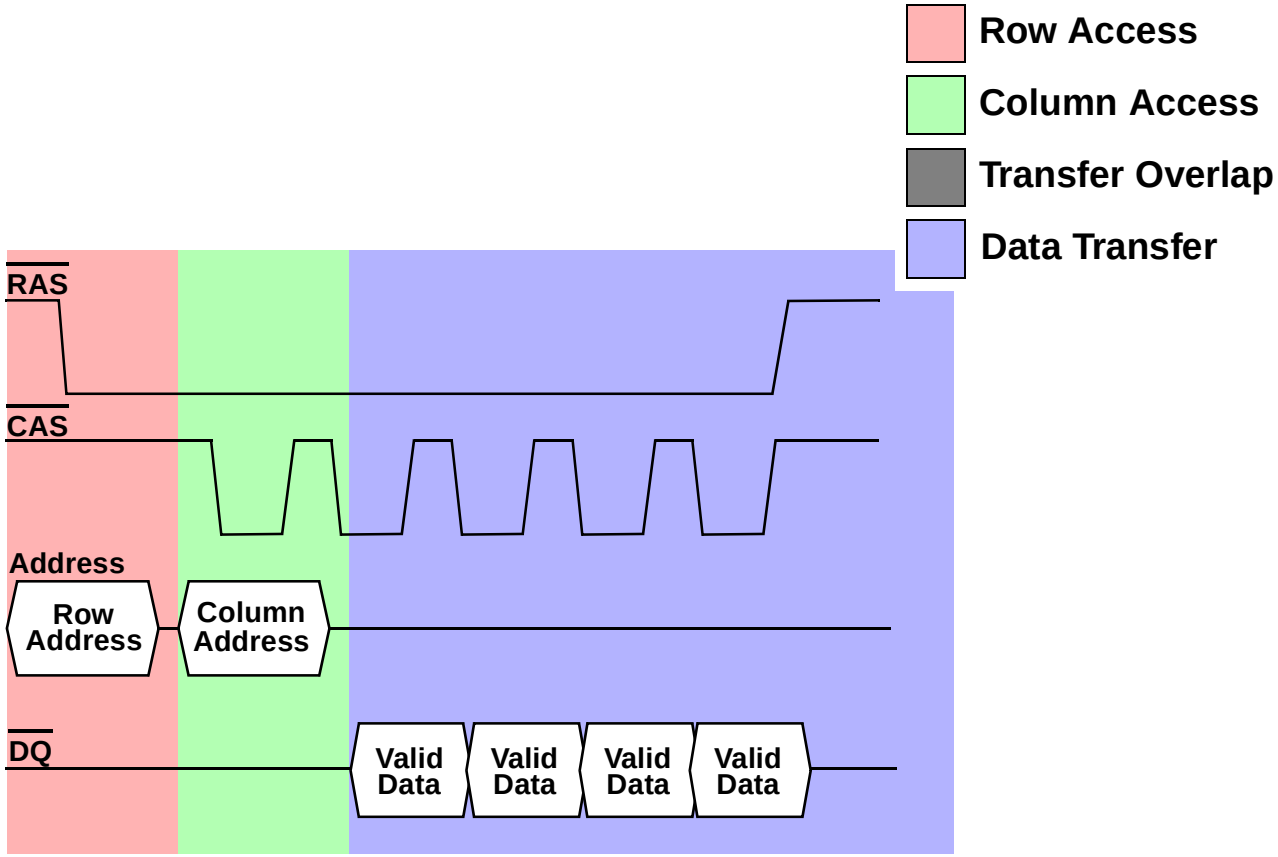
Read Timing for Burst EDO



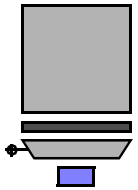
DRAM Evolution



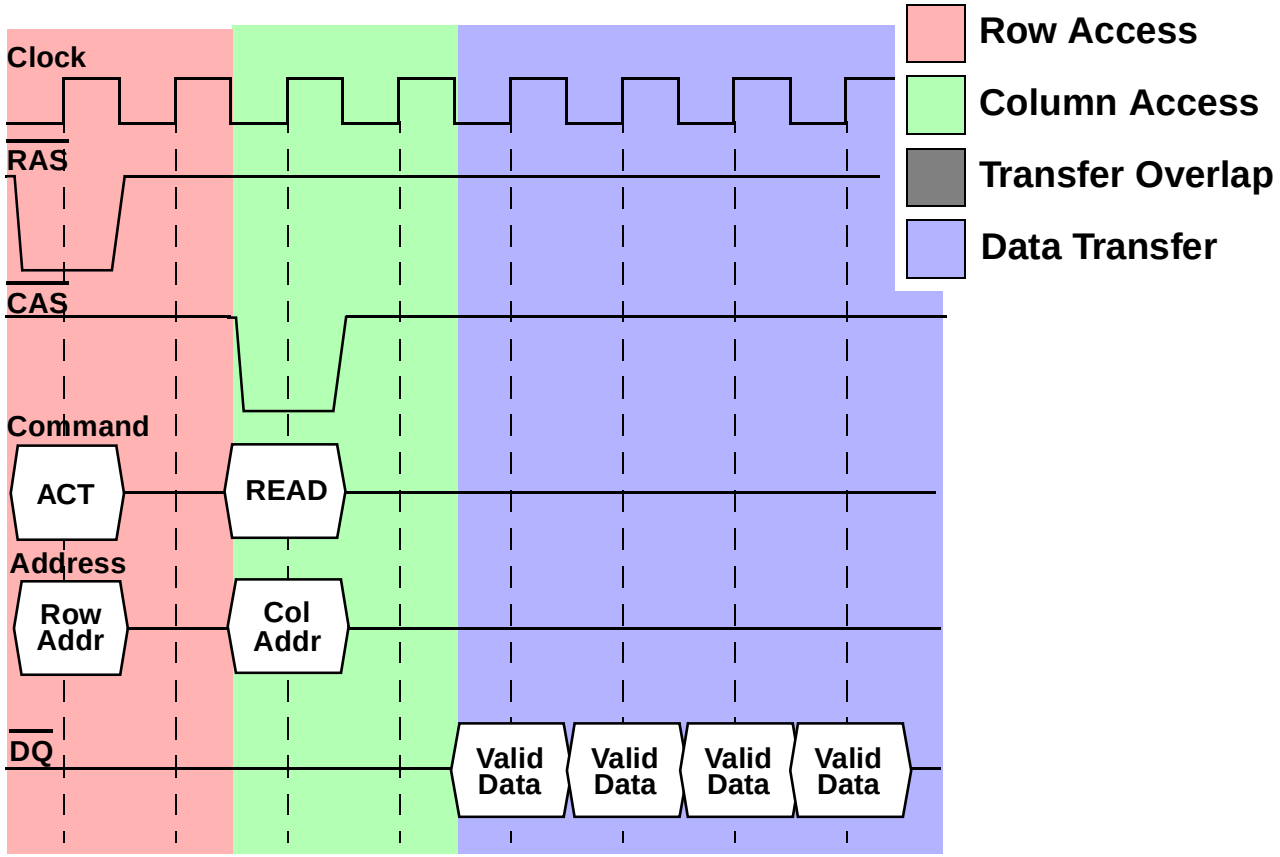
Read Timing for Pipeline Burst EDO



DRAM Evolution

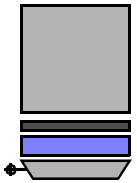


Read Timing for Synchronous DRAM



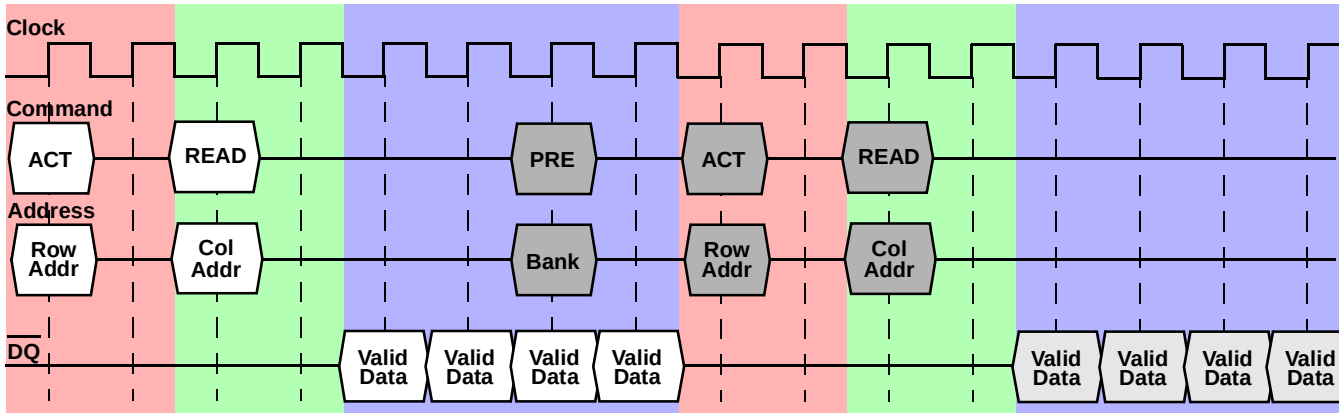
$\overline{(RAS + CAS + OE}$ ... == Command Bus)

DRAM Evolution

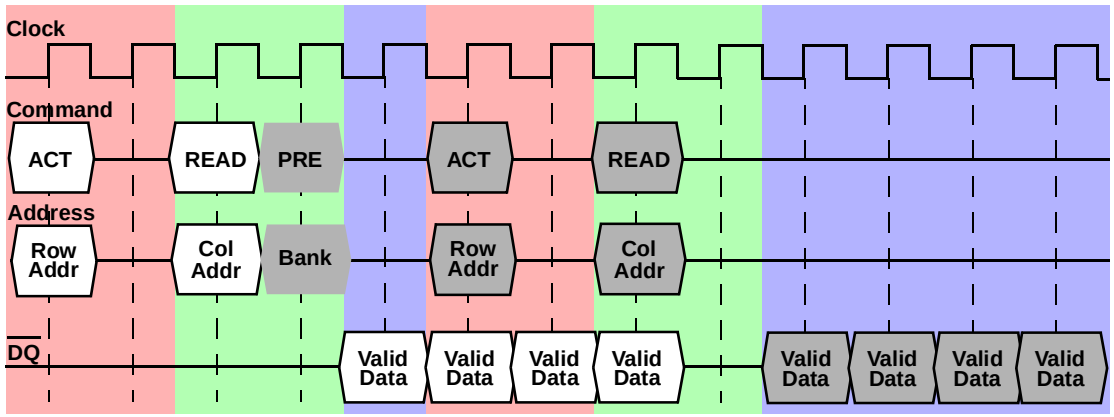


Inter-Row Read Timing for ESDRAM

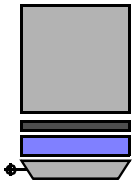
"Regular" CAS-2 SDRAM, R/R to same bank



ESDRAM, R/R to same bank

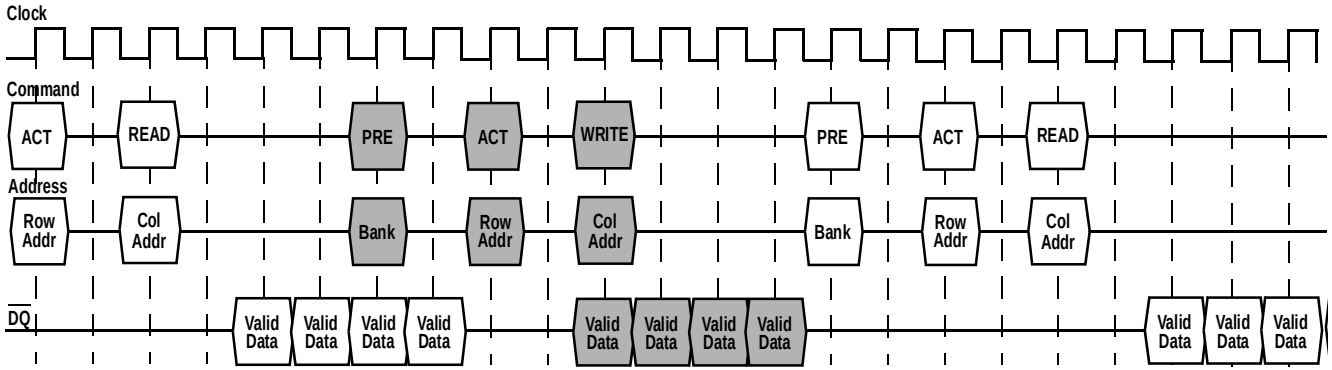


DRAM Evolution

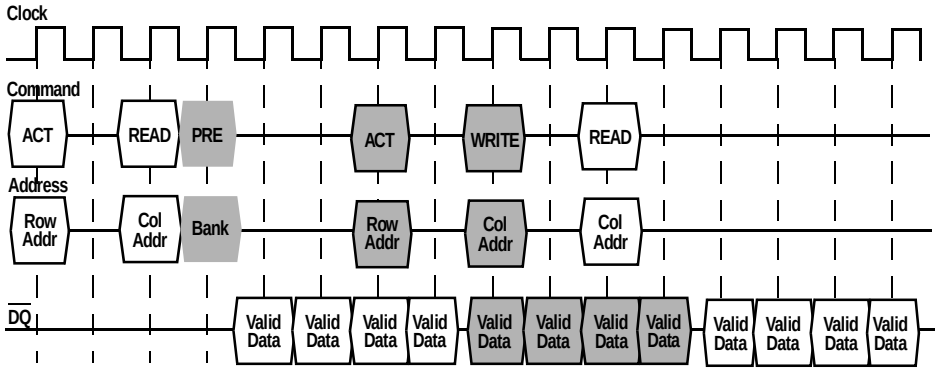


Write-Around in ESDRAM

“Regular” CAS-2 SDRAM, R/W/R to same bank, rows 0/1/0

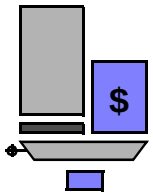


ESDRAM, R/W/R to same bank, rows 0/1/0

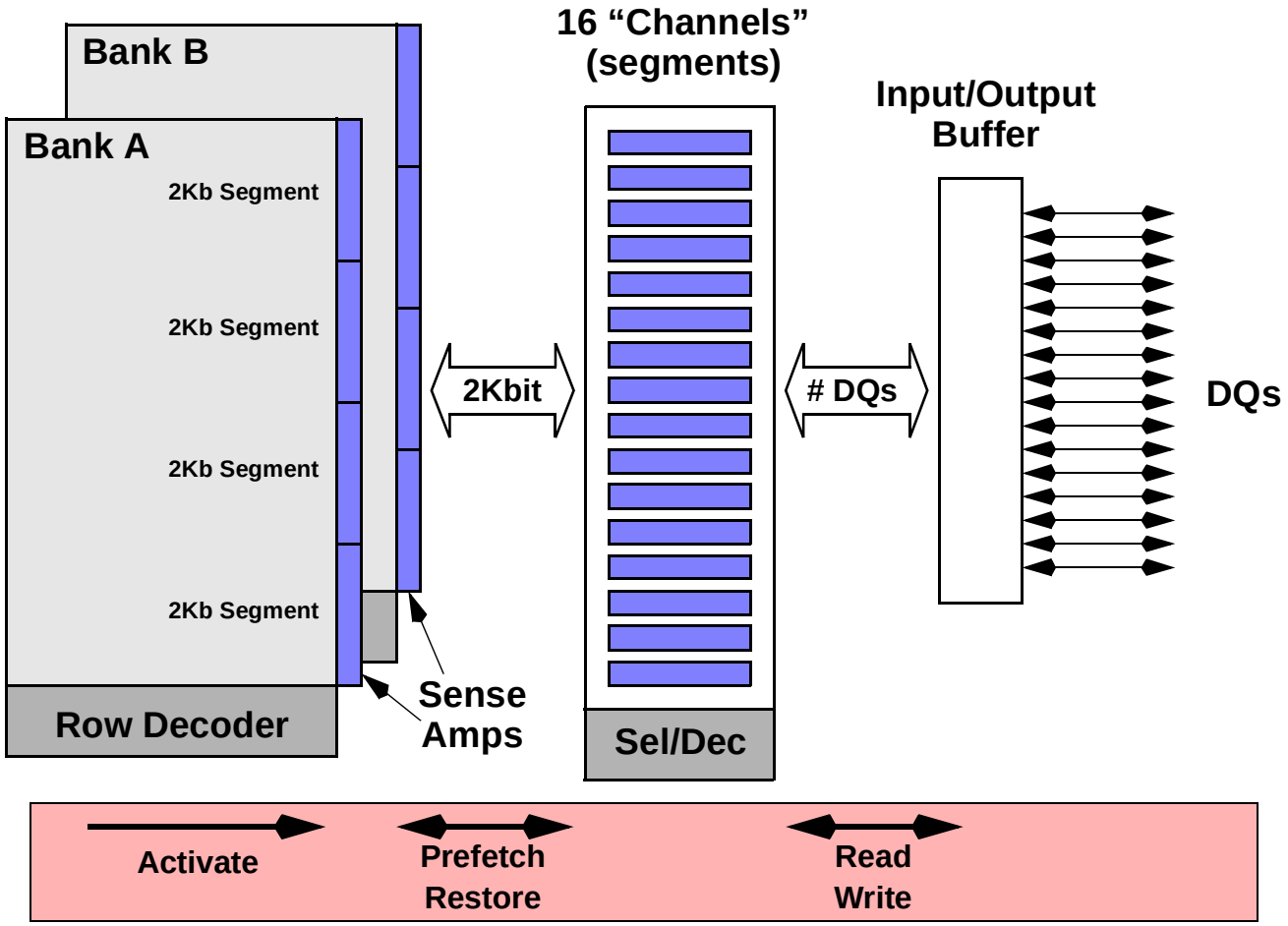


(can second READ be this aggressive?)

DRAM Evolution

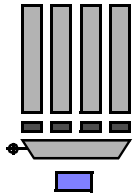


Internal Structure of Virtual Channel

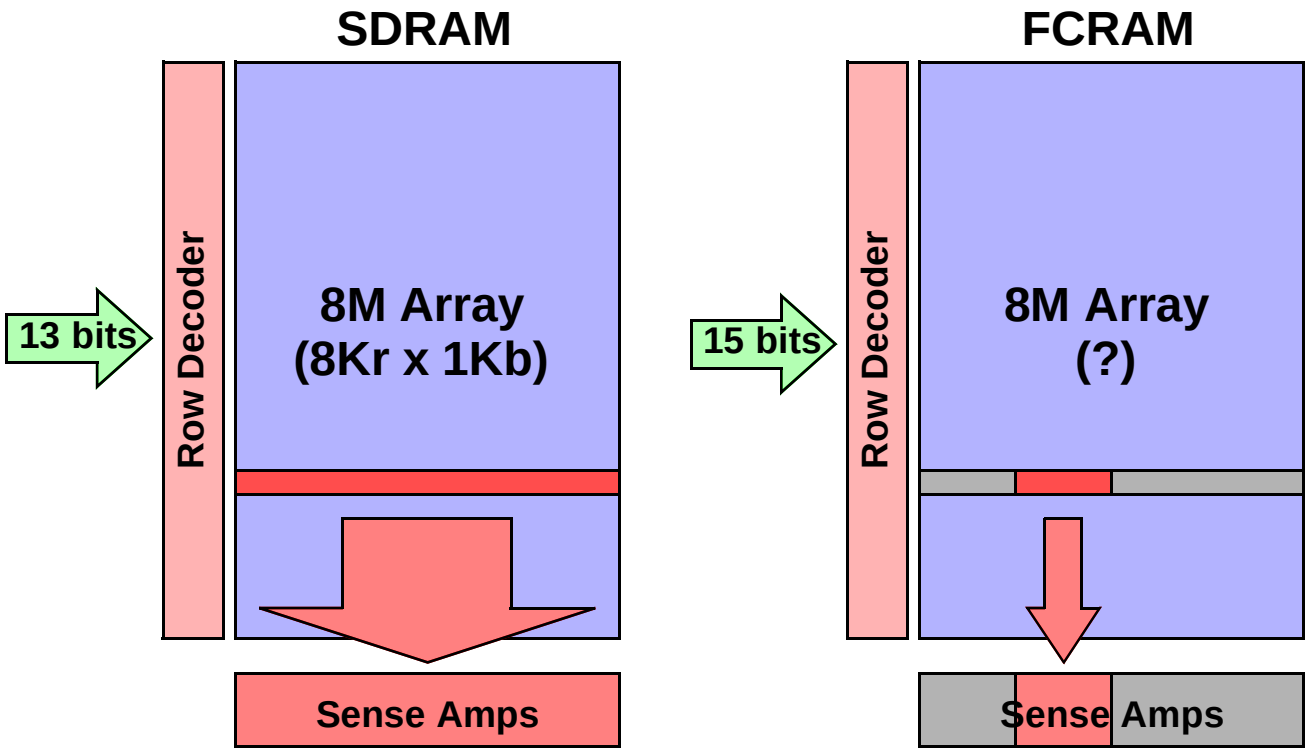


Segment cache is software-managed, reduces energy

DRAM Evolution



Internal Structure of Fast Cycle RAM

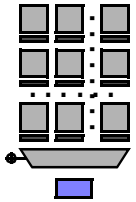


t_{RCD} = 15ns
(two clocks)

t_{RCD} = 5ns
(one clock)

Reduces access time and energy/access

DRAM Evolution



Internal Structure of MoSys 1T-SRAM