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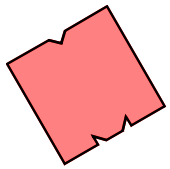
ECE Dept.

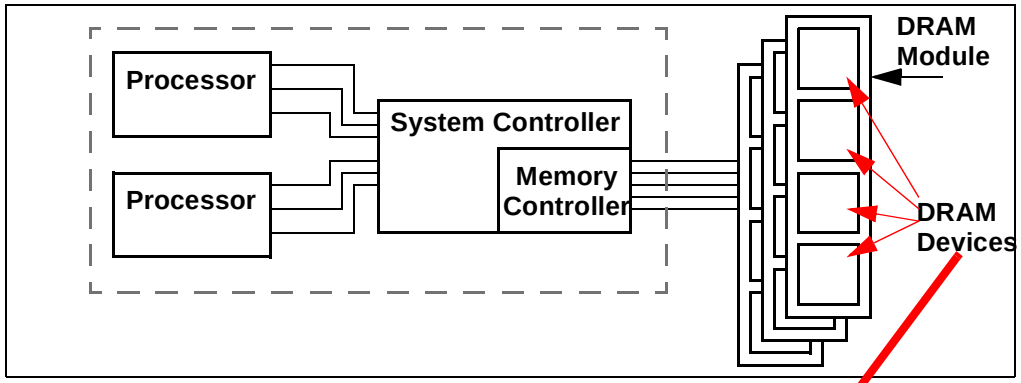
ENEE 759H, Spring 2005
Memory Systems: Architecture and Performance Analysis

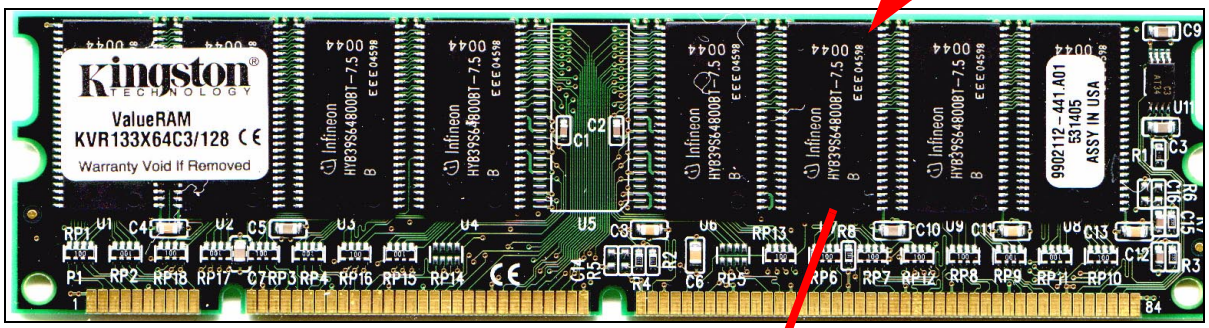
DRAM Device Circuits and Architecture

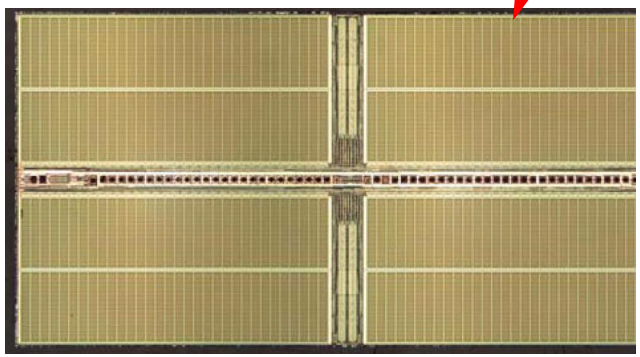
Credit where credit is due:
Slides contain original artwork (© Jacob, Wang 2005)



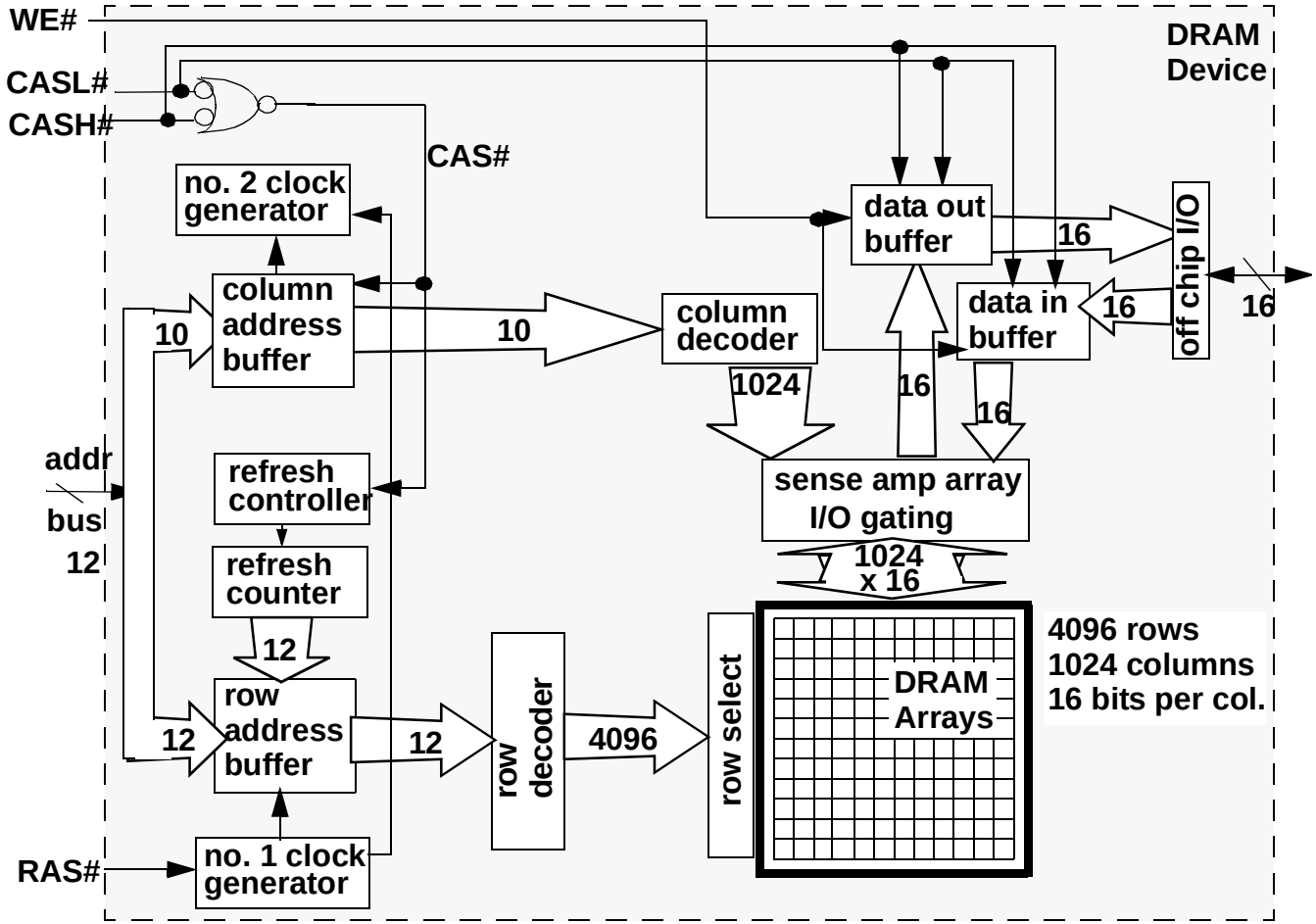
Overview


Processor
Processor
System Controller
Memory Controller
DRAM Module
DRAM Devices


Kingston
TECHNOLOGY
ValueRAM
KVR133X64C3/128
Warranty Void If Removed



DRAM Device Architecture



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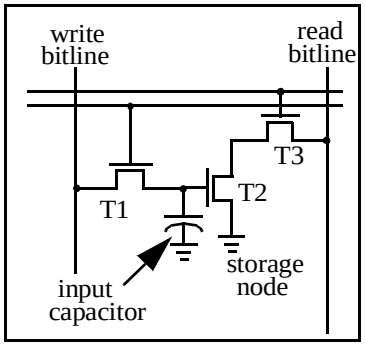
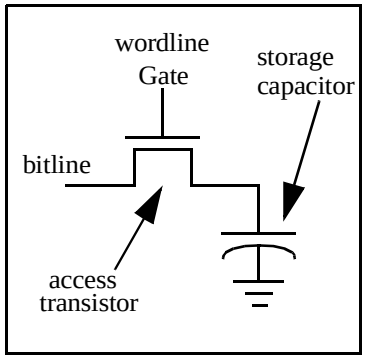
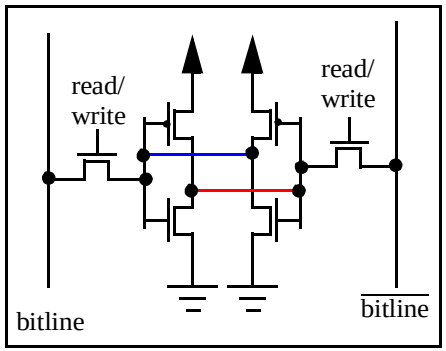
Storage Cells



3T1C storage cell



1T1C storage cell (classic DRAM)



6T storage cell (classic SRAM)

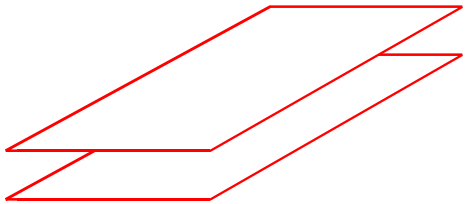
DRAM: Dynamic Random Access Memory

How long does “memory storage” last?

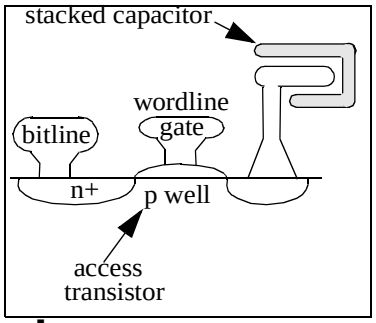
Cell capacitance vs Leakage current

Storage Cell Structure I

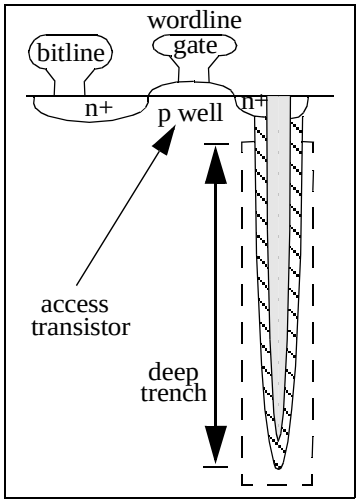
plate capacitor



$$C = \varepsilon \frac{A}{d}$$

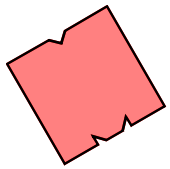


above silicon in poly

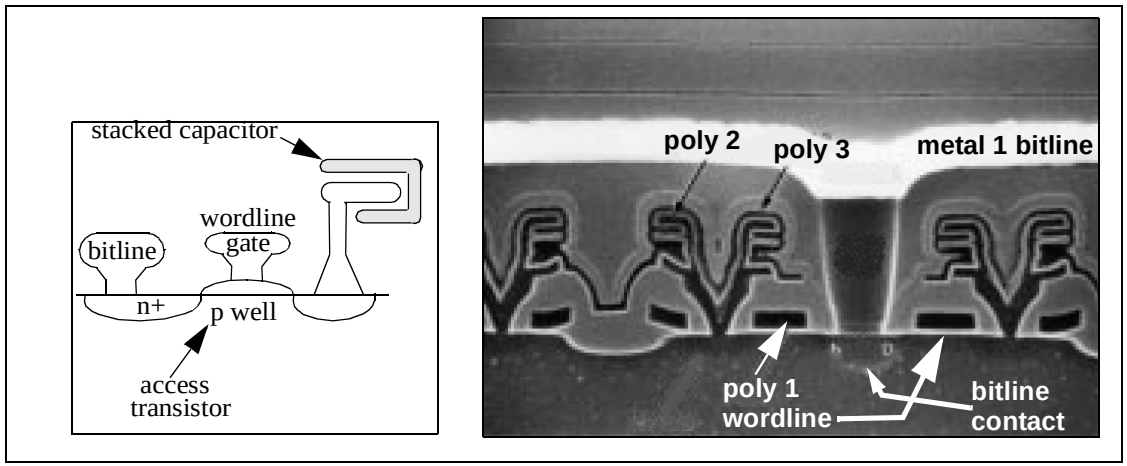


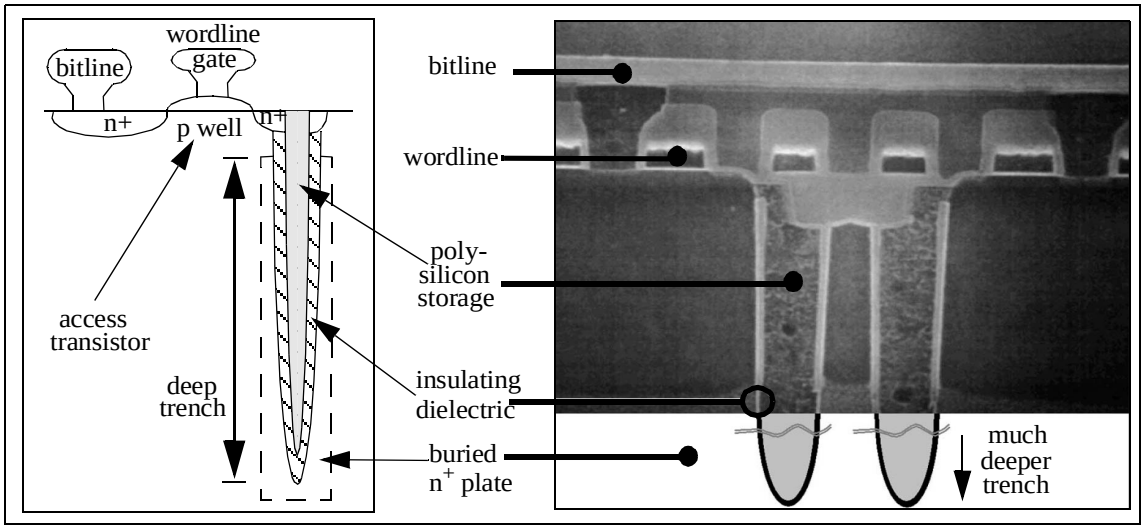
below silicon surface in trench

Shrinking DRAM devices means reduced cross section (area)

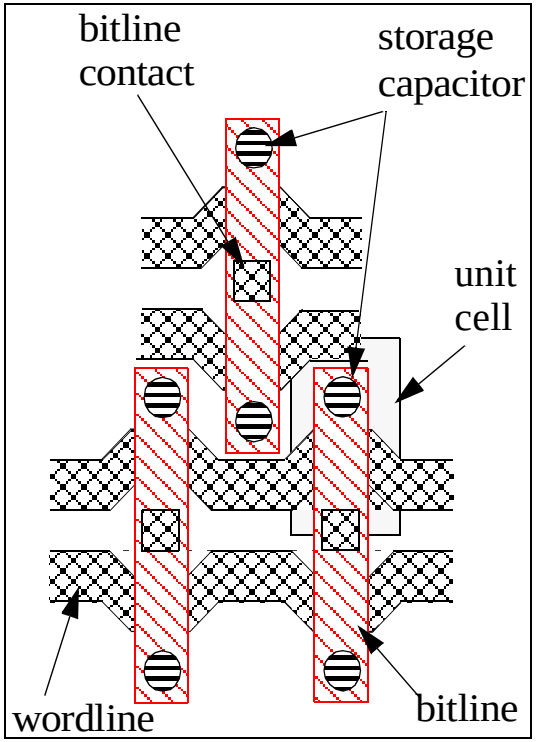


Storage Cell Structure II



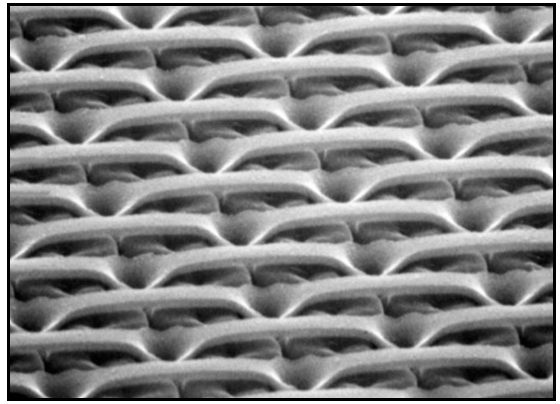


DRAM Array I

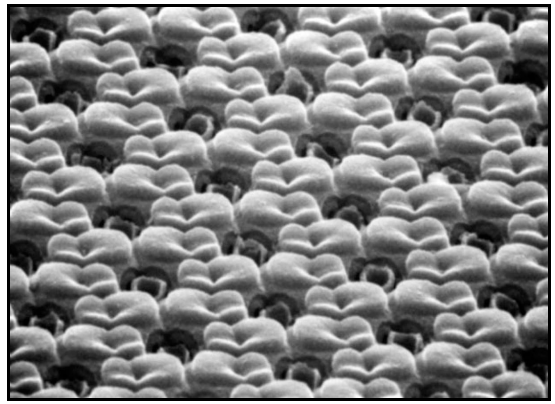


$8F^2$ cell

(F = feature size. 90nm etc)

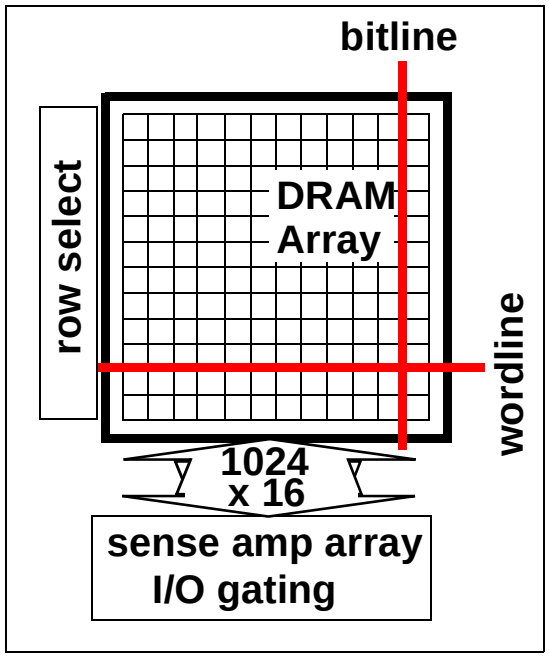


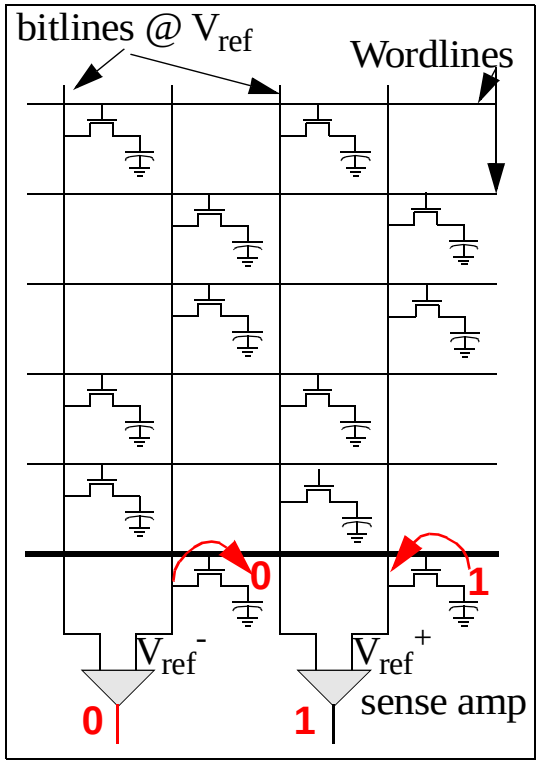
Polycide Bitlines



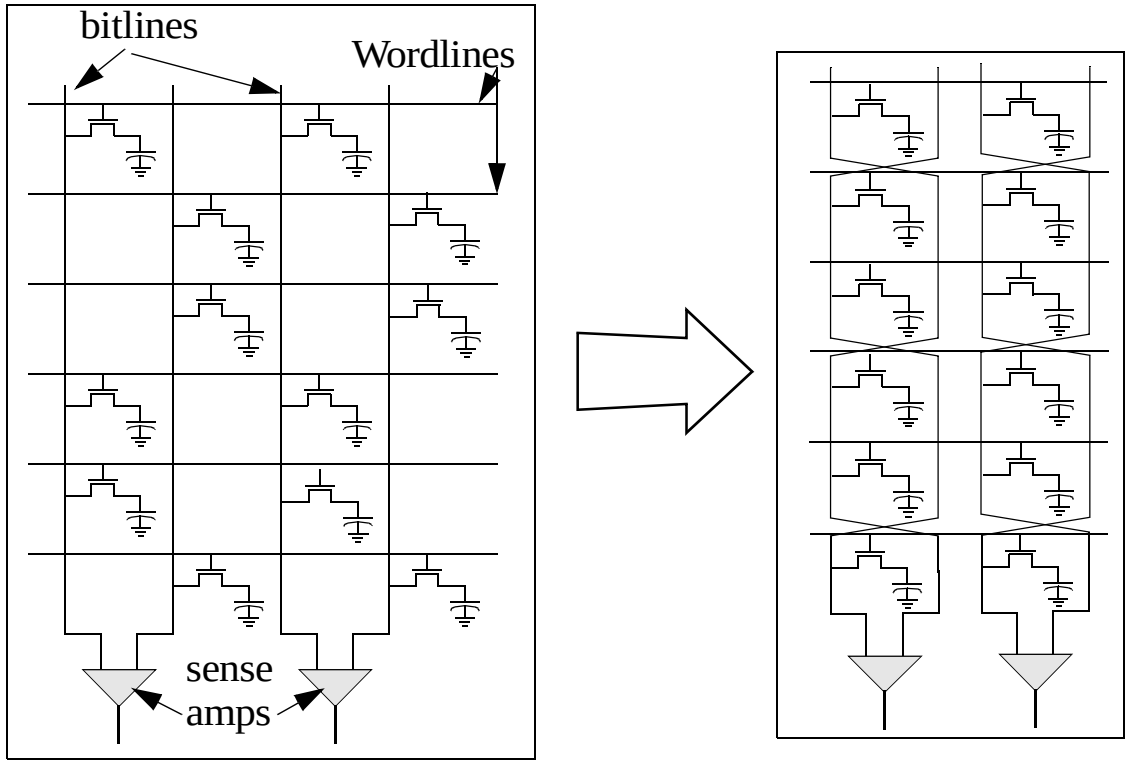
Unlayered DRAM Cell Array

DRAM Array II





DRAM Array III (folded bitline)

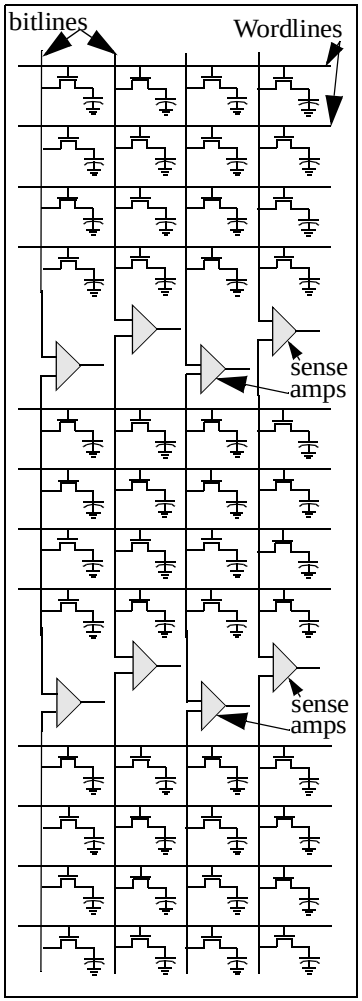


2 Bitline lanes through each cell (larger cell size)

Cell size: typically 8 F^2

Better noise tolerance (common mode rejection)

DRAM Array IV (Open Bitline)



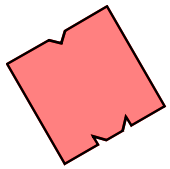
Dummy structures at array edges

1 Bitline lane through each cell

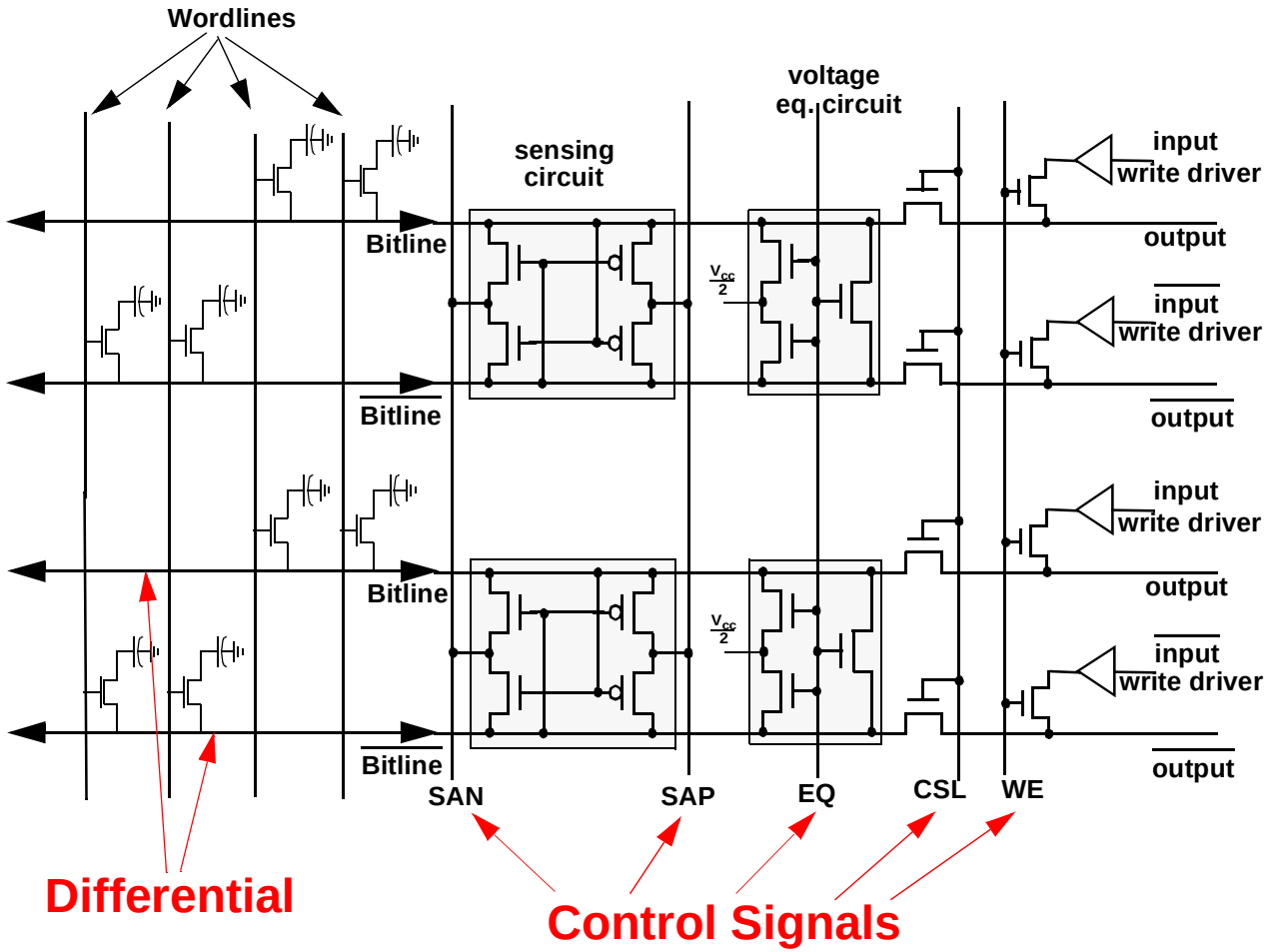
Cell size: typically 6 F^2

Bitline pairs comes from different array segments

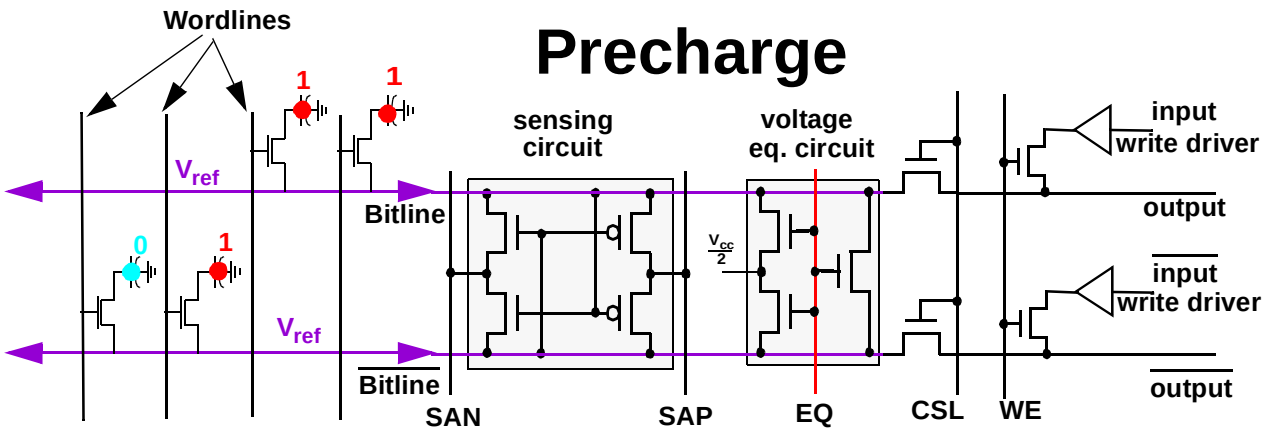
Challenge: How to get good noise tolerance AND small cell size?



Sense Amplifier



Array Precharge

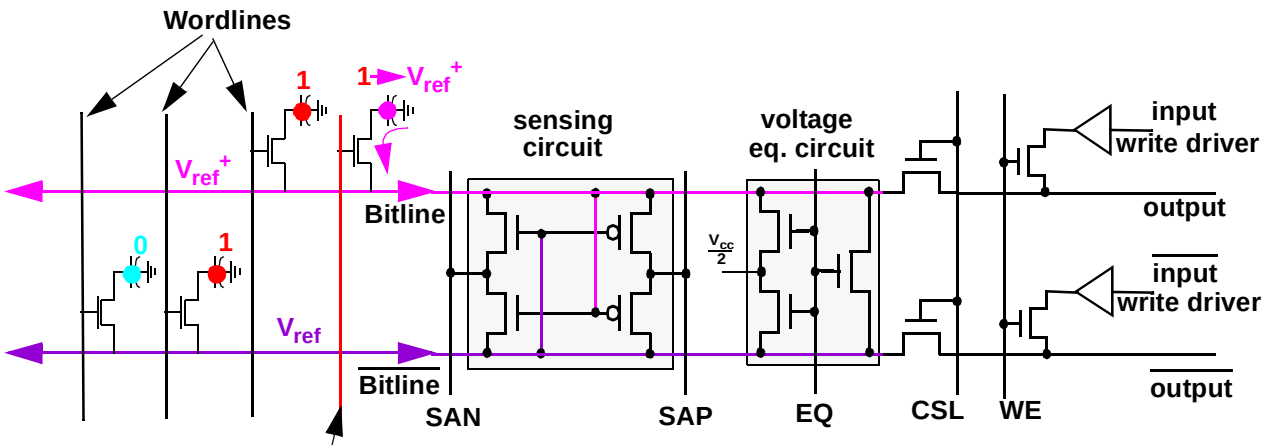


Assert equalize, Array precharged to V_{ref} (typically $V_{cc}/2$)

0 V_{ref}^- V_{ref} V_{ref}^+ 1

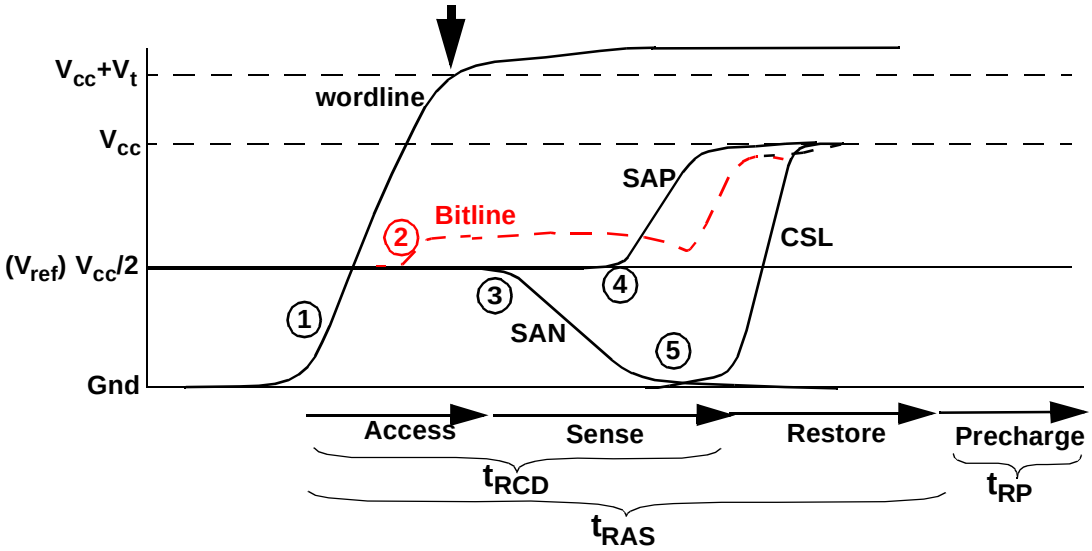
Voltage color chart

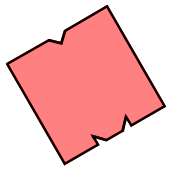
Row Access I



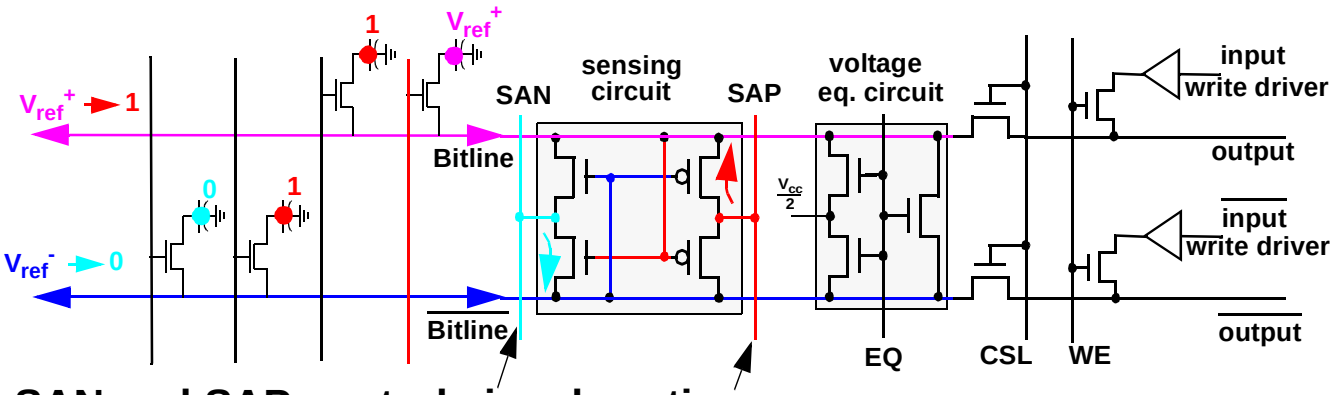
selected row (wordline) activated

timeline





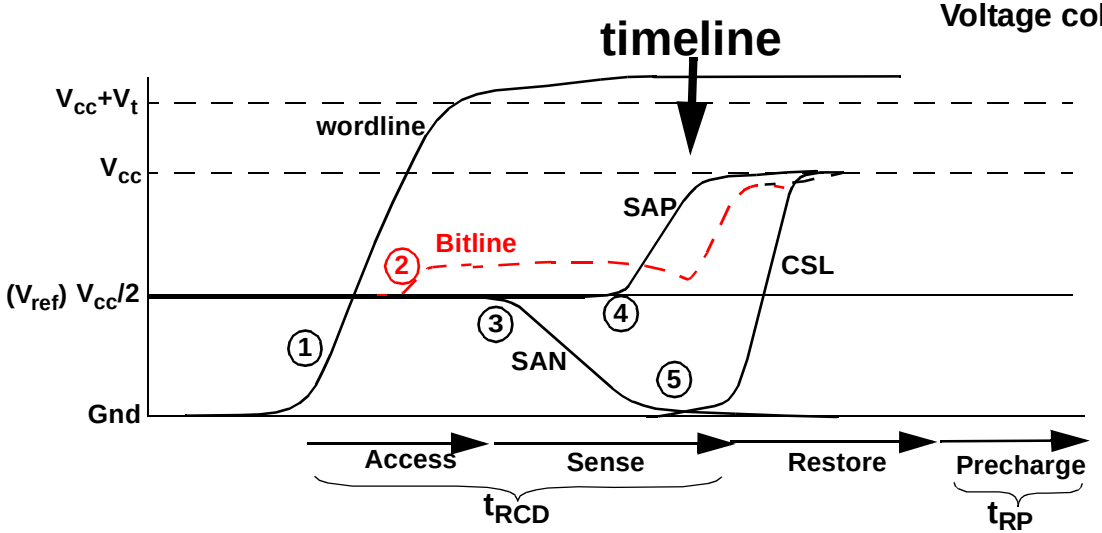
Row Access II (sense)

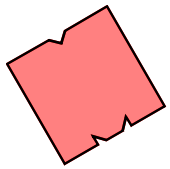


SAN and SAP control signals active lower NFet more conductive, upper PFet more conductive. Bitline pairs slammed to opposite voltage rails, then upper NFet and lower PFet shut off completely.

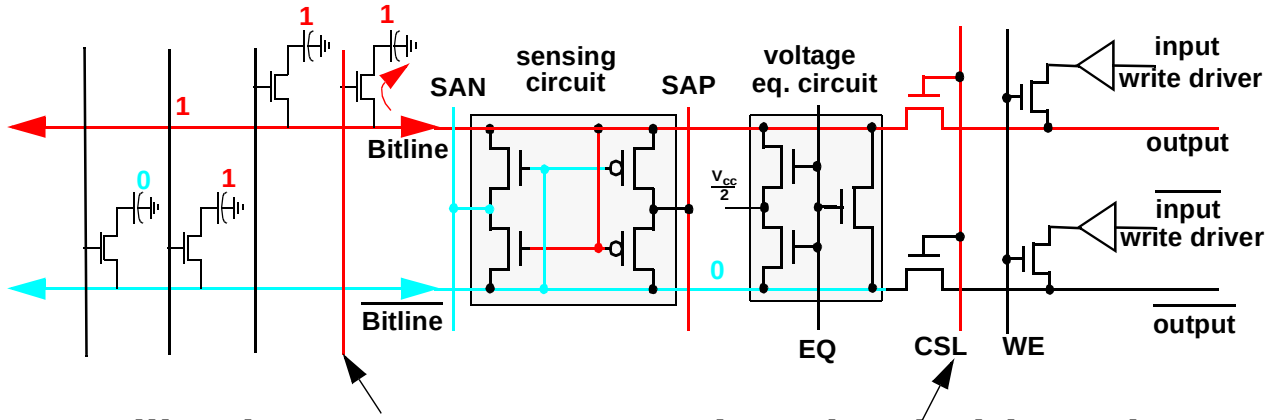
0 V_{ref}^- V_{ref} V_{ref}^+ 1

Voltage color chart





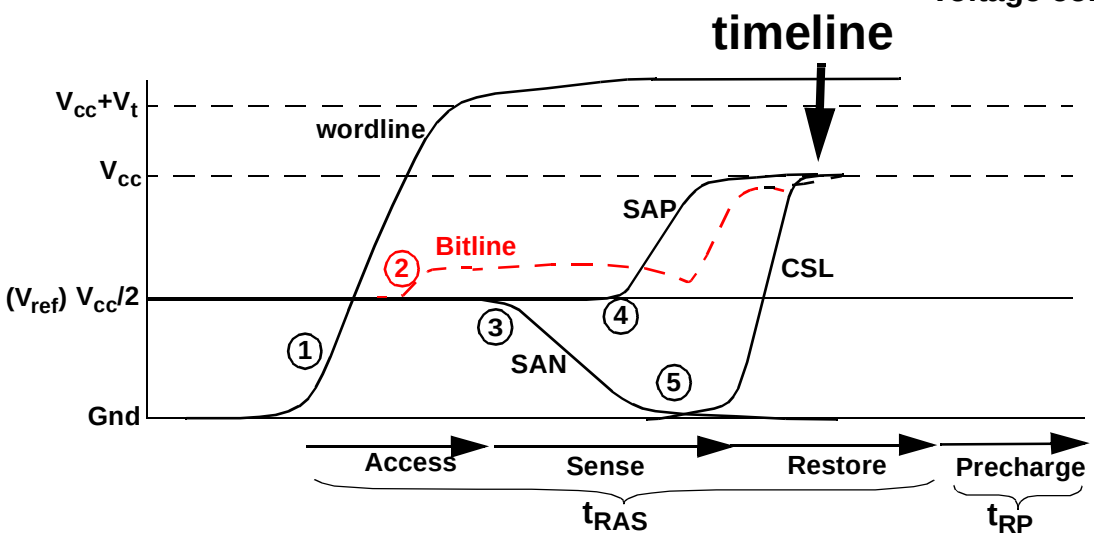
Row Access III (Restore)



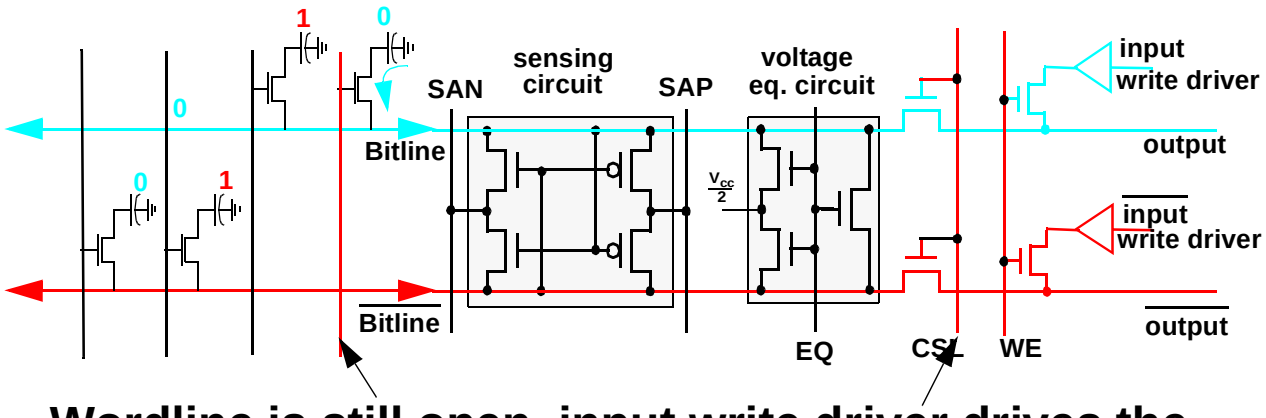
Wordline kept open, now sensing circuit drives the full voltage level "1" back into cell. If the column is selected, data is driven out to rest of the world.

0 V_{ref}^- V_{ref} V_{ref}^+ 1

Voltage color chart



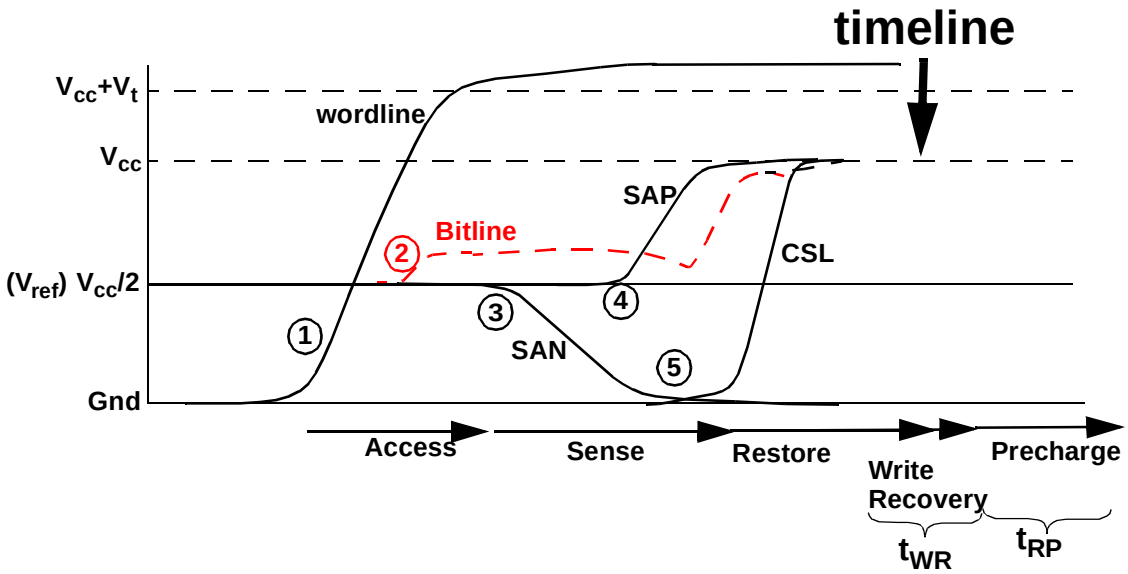
Write (over old data)

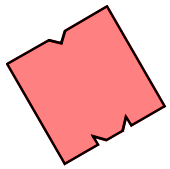


Wordline is still open, input write driver drives the full voltage level "0" into cell.

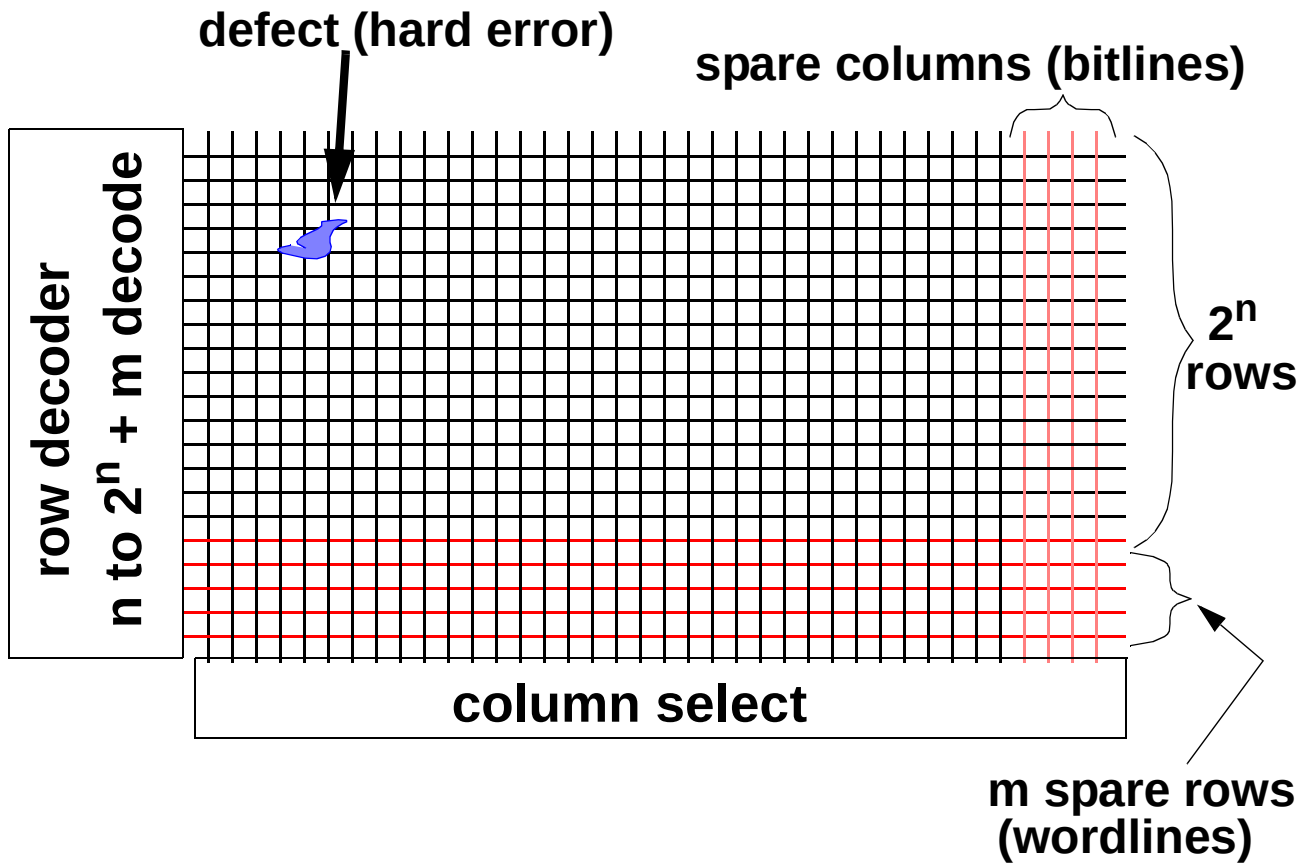
0 V_{ref}^- V_{ref} V_{ref}^+ 1

Voltage color chart



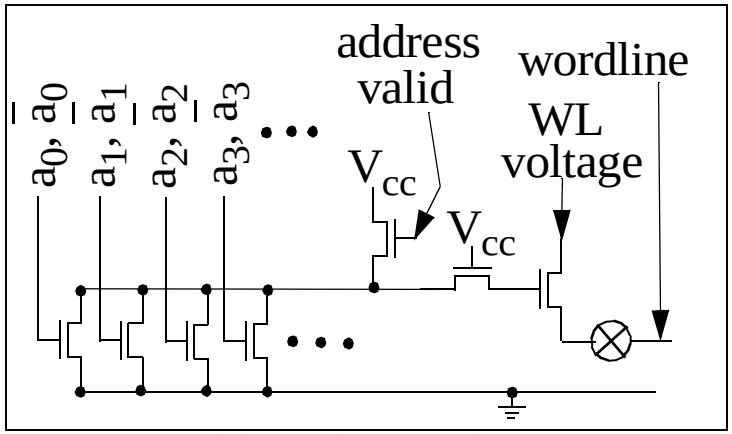


Decoders and Redundancy

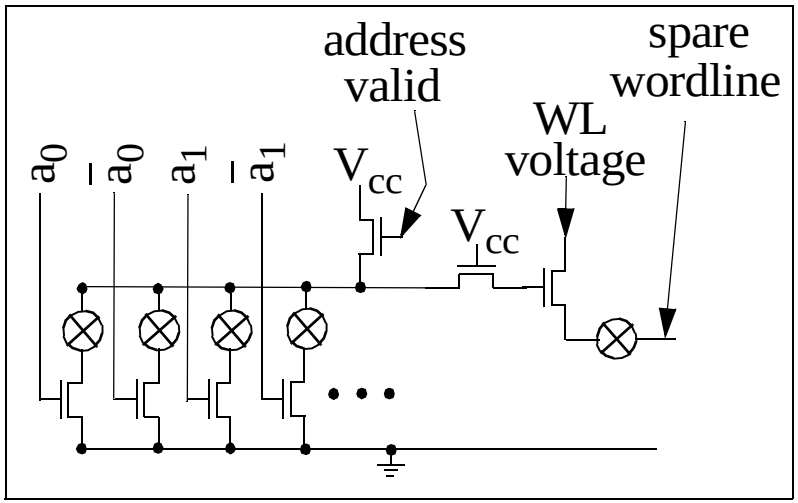


Challenge: How to get good yield and tolerate *some* defect?

Programmable Decoders I

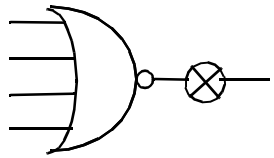


standard decoder (each row has one)

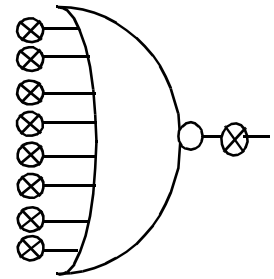


spare decoder (each spare row has one)

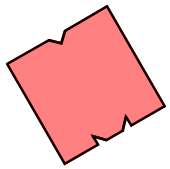
⊗ (laser) programmable link



functionally equivalent to NOR gate with output that can be disabled by laser (or fuse)

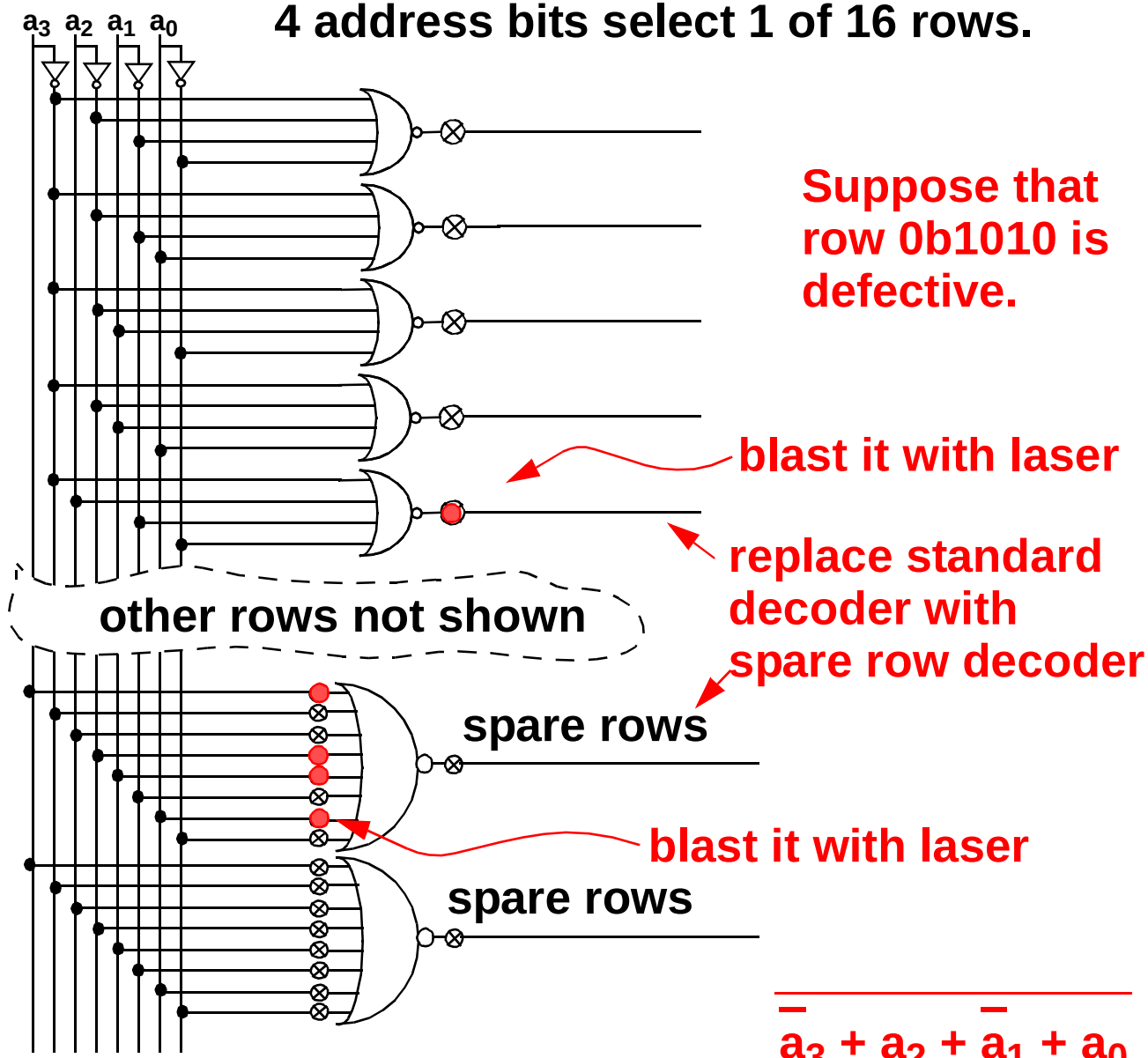


functionally equivalent to NOR gate with inputs that can be selectively disabled

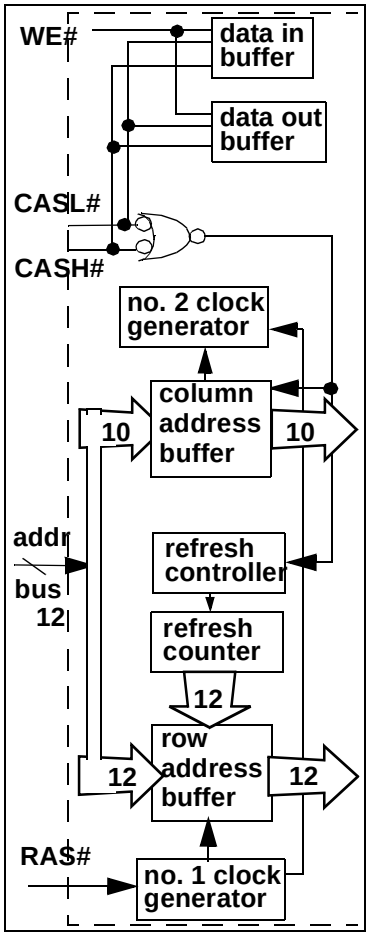


Programmable Decoders II

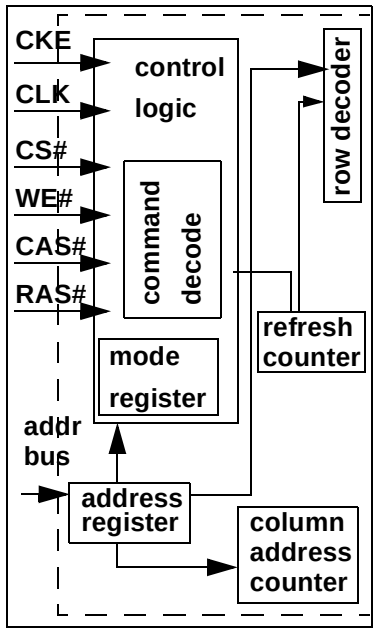
4 address bits select 1 of 16 rows.



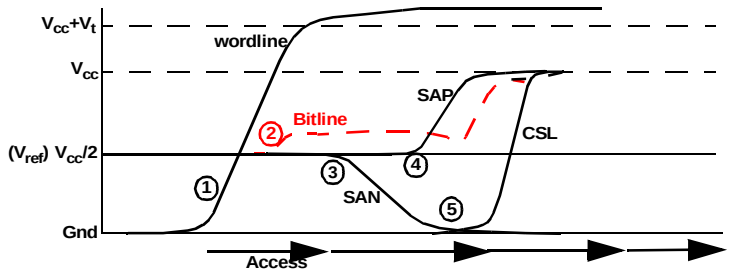
Device Control Logic

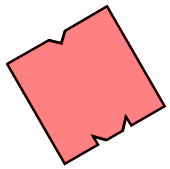


SDRAM Control Logic FPM

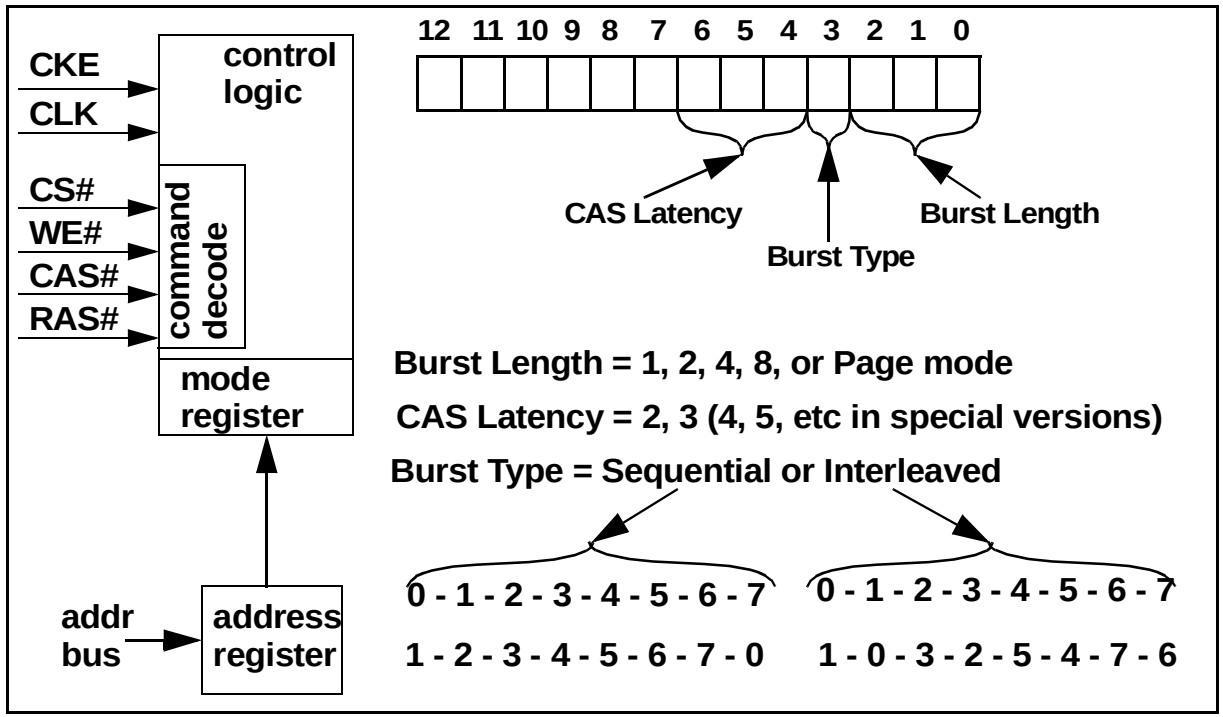


Remember SAN and SAP? Something has to control sequence and timing



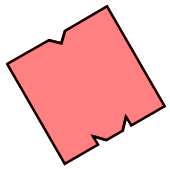


Mode Register

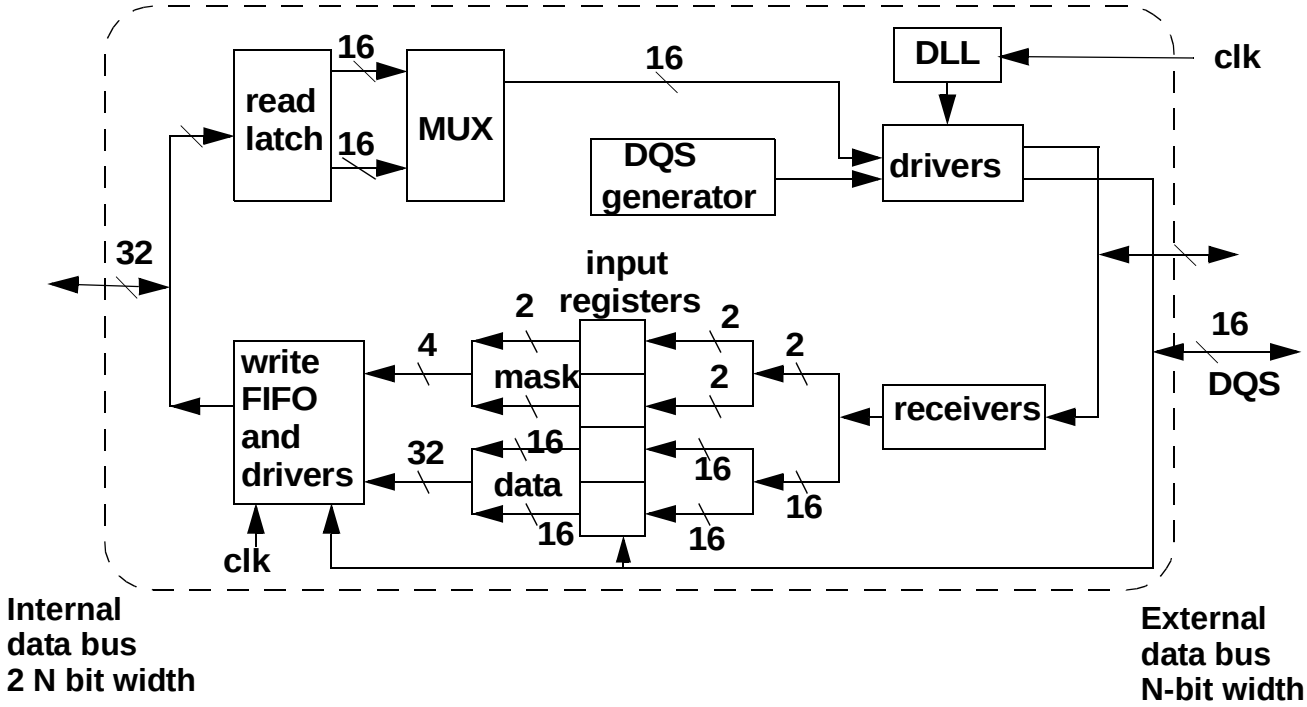


Modern DRAM devices (SDRAM, Direct RDRAM, DDRx SDRAM, etc. have programmable behaviour)

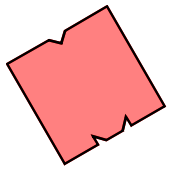
Load value from address bus with special command.



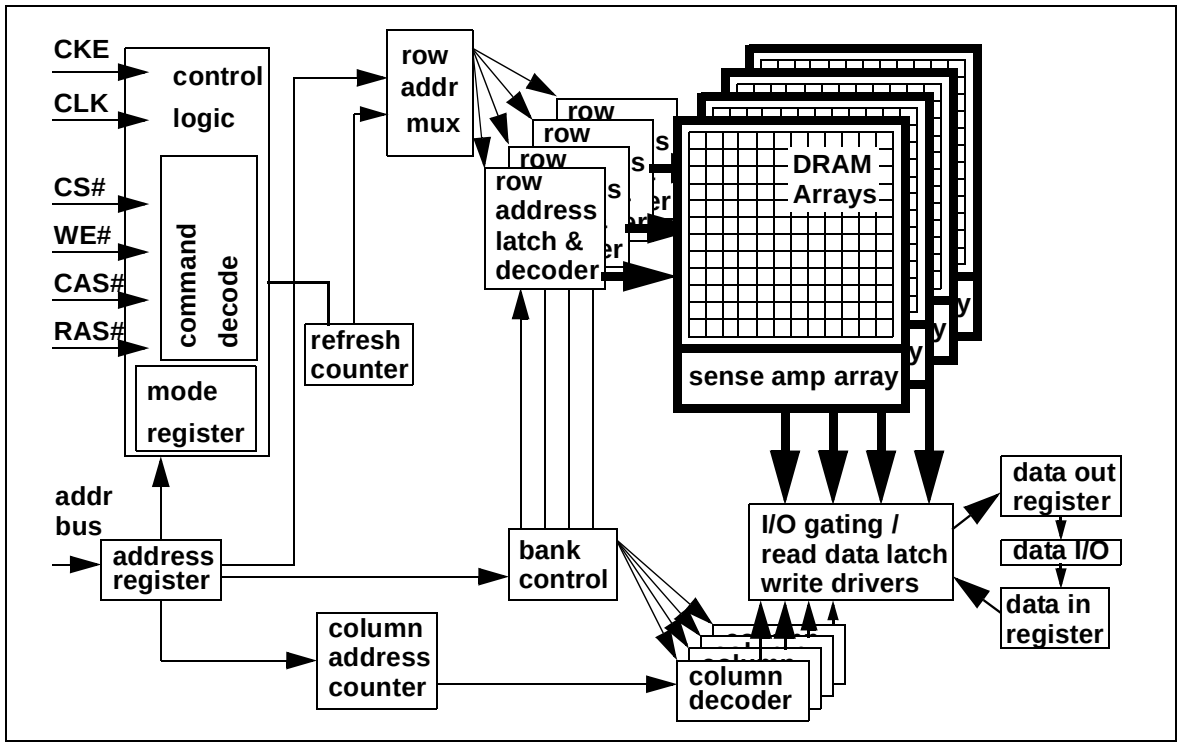
Data I/O

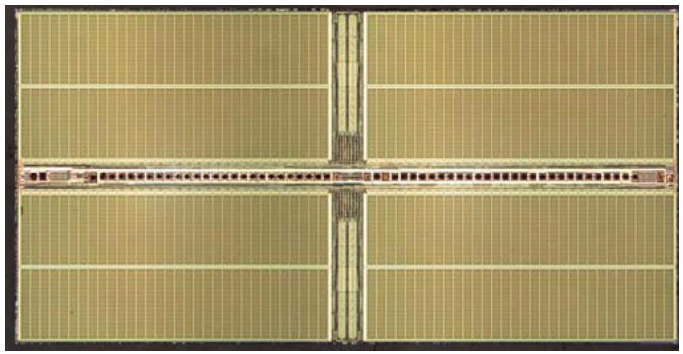


2N Bit prefetch in DDR SDRAM devices
4N in DDR2 SDRAM devices, and
8N in DDR3 SDRAM devices
Allows "core" to run at slower datarates while interface datarate cranks up.
drawback - minimum burst lengths (loss of "randomness")

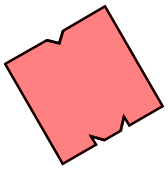


SDRAM Device





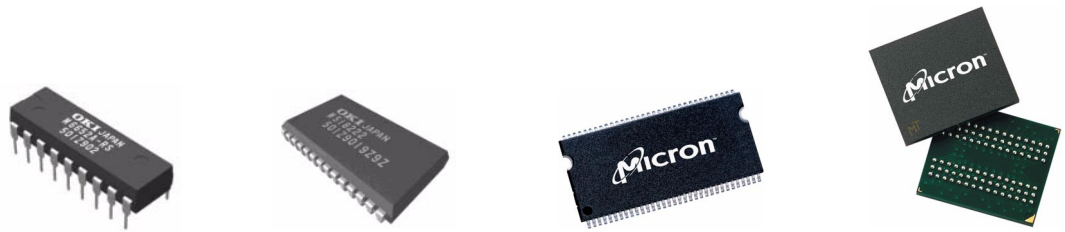
Find bank 0, row 0x02F1, column 0x0EA and get an A



Package and Pincount I

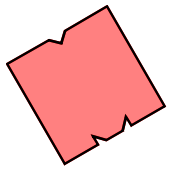
	2004	2007	2010	2013	2016
Semi Generation (nm)	**90**	**65**	**45**	**32**	**22**
High Perf. device pin count	**2263**	**3012**	**4009**	**5335**	**7100**
High Perf. device cost (cents/pin)	**1.88**	**1.61**	**1.68**	**1.44**	**1.22**
Memory device pin count	**48-160**	**48-160**	**62-208**	**81-270**	**105-351**
Memory device pin cost (cents/pin)	**0.34 - 1.39**	**0.27 - 0.84**	**0.22 - 0.34**	**0.19 - 0.39**	**0.19 - 0.33**

ITRS Roadmap

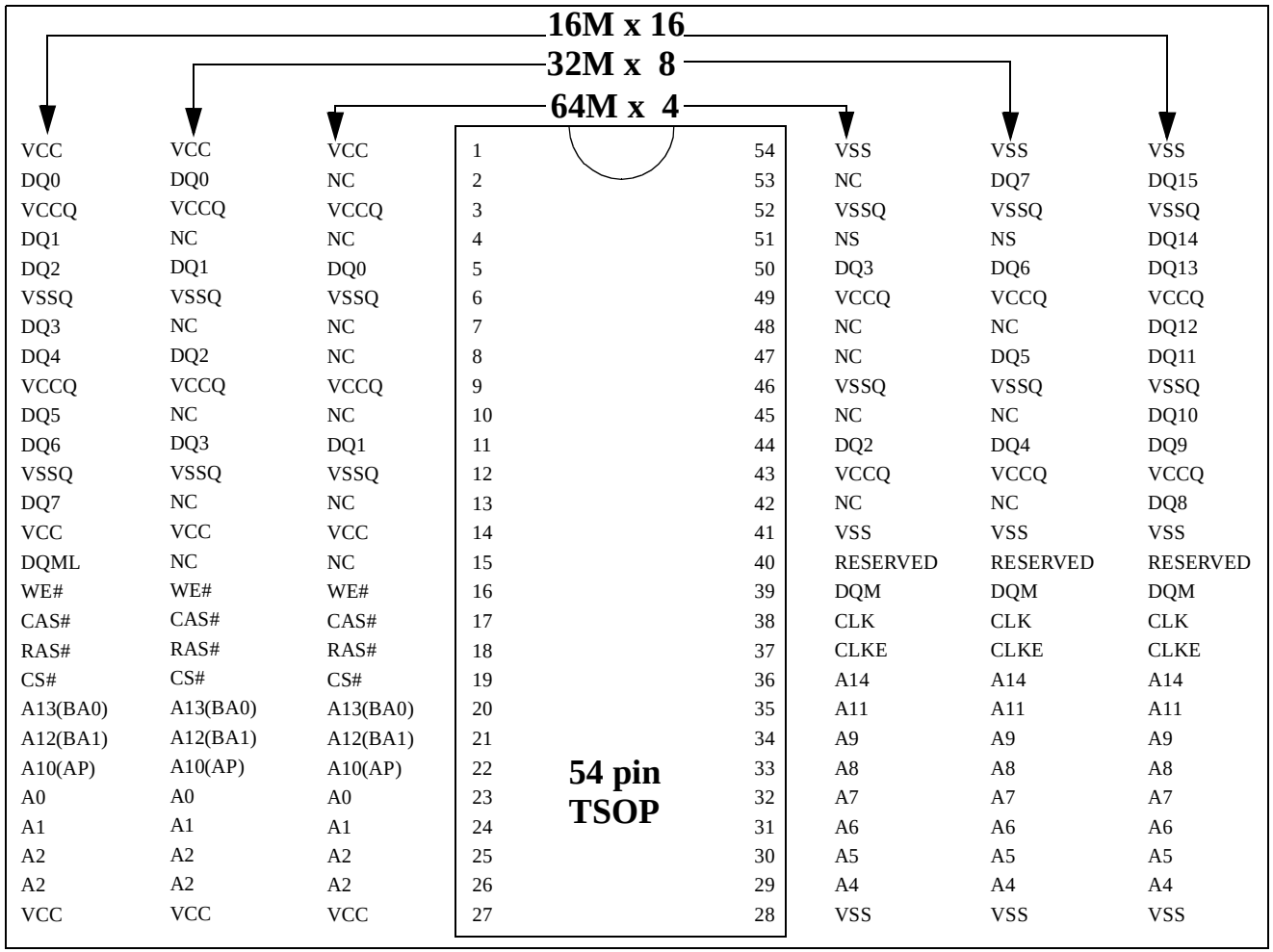


DIP **SOJ** **TSOP** **BGA**

Package Evolution
(higher pin count, higher datarate)
(higher costs, testing etc.)

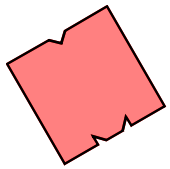


Package and Pincount II



16M x 16	32M x 8	64M x 4		16M x 16	32M x 8	64M x 4
VCC	VCC	VCC	1	VSS	VSS	VSS
DQ0	DQ0	NC	2	NC	DQ7	DQ15
VCCQ	VCCQ	VCCQ	3	VSSQ	VSSQ	VSSQ
DQ1	NC	NC	4	NS	NS	DQ14
DQ2	DQ1	DQ0	5	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6	VCCQ	VCCQ	VCCQ
DQ3	NC	NC	7	NC	NC	DQ12
DQ4	DQ2	NC	8	NC	DQ5	DQ11
VCCQ	VCCQ	VCCQ	9	VSSQ	VSSQ	VSSQ
DQ5	NC	NC	10	NC	NC	DQ10
DQ6	DQ3	DQ1	11	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12	VCCQ	VCCQ	VCCQ
DQ7	NC	NC	13	NC	NC	DQ8
VCC	VCC	VCC	14	VSS	VSS	VSS
DQML	NC	NC	15	RESERVED	RESERVED	RESERVED
WE#	WE#	WE#	16	DQM	DQM	DQM
CAS#	CAS#	CAS#	17	CLK	CLK	CLK
RAS#	RAS#	RAS#	18	CLKE	CLKE	CLKE
CS#	CS#	CS#	19	A14	A14	A14
A13(BA0)	A13(BA0)	A13(BA0)	20	A11	A11	A11
A12(BA1)	A12(BA1)	A12(BA1)	21	A9	A9	A9
A10(AP)	A10(AP)	A10(AP)	22	A8	A8	A8
A0	A0	A0	23	A7	A7	A7
A1	A1	A1	24	A6	A6	A6
A2	A2	A2	25	A5	A5	A5
A2	A2	A2	26	A4	A4	A4
VCC	VCC	VCC	27	VSS	VSS	VSS

SDRAM “Same pinout”, except for data bus



Process Technology