SDR-SDRAM-CTRL

Single Data Rate Mobile SDRAM Controller Core

The SDR-SDRAM-CTRL core provides provides a simplified, burst-optimized interface to all industry-standard Mobile and ordinary SDRAM devices currently on the market. The distinctive characteristics of the particular core are:

Simplicity of use. All management and initialization procedures are done by the core. Furthermore, all required address, page and burst handling procedures are hidden from the user.

Flexibility. All memory parameters are runtime configurable. The core can be configured in real time, to support literally all SDR devices on the market (from one 16Mbit device up to eight 512Mbit devices, or up to four 2GByte DIMMs, Mobile or not, fast or slow).

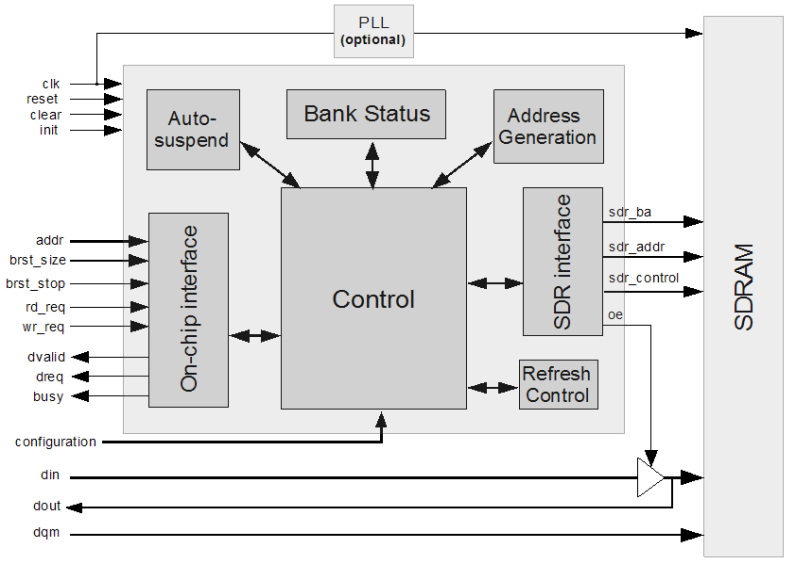
Performance. Pipelining and parallel-state-machines design practices achieve maximal bandwidth utilization.

The SDR-SDRAM-CTRL core provides a simple and easy-to-use user interface, with separate read and write ports. It allows for single word accesses as well as arbitrary length bursts emulating a linear memory space with no page or bank boundaries.

Applications

- Any application requiring efficient, high performance access SDRAM memory
- Processor Interfaces
- Networking
- Video / Image Processing

Block Diagram



Features

- Supports up to 2G address space, 1 to 8 chip-selects, 2 to 4 banks, 11 to 14 row bits and 8 to 12 columns bits.
- Supports all standard SDRAM chips and registered/unbuffered DIMMs.
- Access cascading and efficient back management enable up to 100% utilization of the memory throughput.
- Programmable auto-refresh policy, in order to minimize overhead.
- Runtime-configurable timing parameters (CAS latency, tRP, tRCD, tREFC, tMRD, …).
- Runtime-configurable memory settings (Row bits, Column bits, Bank bits, number of CSs).
- Runtime configurable Mobile-SDR support and Extended-Mode-Register (EMR) values.
- Bank status monitoring. Banks are opened or closed only when necessary, minimizing access delays.
- Configurable auto-close mechanism that precharges inactive banks, in order to minimize power-dissipation.
- Configurable auto power-down and auto-self-refresh.
- Supports sleep-mode.
- Flexible user-interface, with separate read and write interfaces that can support from single to any arbitrary length burst accesses.
- Can be easily interfaced to legacy on-chip synchronous microprocessor busses that support burst-accesses and handshaking or to on-chip FIFOs.

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Functional Description

The SDR-SDRAM-CTRL core performs all initialization and refresh procedures in order for the SDRAM to be setup correctly and to ensure data integrity. After the initial delay required by the SDRAM devices, has elapsed, the required initialization procedure commences depending on the type of SDRAM (mobile or not). Once initialization is complete, the controller can accept read and write requests. The requests are served in a first-come-first-served policy. The controller checks whether the particular memory location can be directly accessed or bank-precharge and/or bank-activate is required. After sending the required command sequences, the controller then informs either that valid data exists on the dout-bus or that data is required on the din-bus. Due to the pipelined architecture of the controller, required pre-charge/activate operations, are issued while performing read or write. The controller can be configured to automatically precharge activated banks after some time of inactivity. In that case the respective pre-charge commands are performed without obstructing ongoing read/write processes.

The SDR-SDRAM-CTRL core has an automatic power-down and suspend mechanism, that puts the SDRAM device into power-down mode after a programmable time of inactivity. If a read/write request is issued, the controller “wakes-up” right away and serves the request. The controller also wakes-up to serve an internal auto-refresh request and then returns to power-down mode again. After an additional time of inactivity the controller enters into suspend mode, where the SDRAM device is put into self-refresh mode and most of the internal circuitry is frozen. When a read or write request is issued, the controller performs the required steps for the device to exit the self-refresh mode and then serves the request.

The SDR-SDRAM-CTRL core provides run-time configuration inputs for controlling many SDRAM parameters, such as: burst-length, timing parameters, address settings (number of row-bits, column bits, etc.), mobile support, mobile EMR values, etc. This ensures compatibility with virtually any SDRAM device on the market.

The SDR-SDRAM-CTRL core incorporates a parallel auto-close mechanism, which precharges active SDRAM banks that are currently inactive. It also incorporates an Auto-Power-Down & Auto-Self-Refresh mechanism which sets the SDRAM device into “power-down” mode after a configurable time of inactivity. When in power-down mode and if a user or auto-refresh request is received, the SDRAM is set back into normal-mode and the request is served. If an additional time of inactivity is observed, the SDRAM device(s) are set into self-refresh mode, during which the internal SDRAM self-refresh mechanism is used. During this mode, most of the internal circuitry is “frozen”, dropping power dissipation to a minimum. And finally, it also takes care of SDRAM refresh requirements.

Implementation Results

The SDR-SDRAM-CTRL core has been evaluated in a variety of technologies. The following Actel results are obtained after speed optimization during synthesis and place and route, without a PHY, while assuming that all core I/Os are routed off-chip.

It must be noted that the SDR-SDRAM-CTRL core in most cases can achieve operating frequencies in excess of 200 MHz. However in order to support SDRAM devices operating at high frequencies (higher than 100Mhz), careful clock distribution is essential. The use of a PLL and/or a clock delay line is required in most cases in order to achieve maximum SDRAM frequencies. The following results correspond to a full-featured SDR-SDRAM-CTRL core, except that it can support only up to two chip-selects.

Actel

Family Device	Cells/Tiles		Ram Blocks	Fmax (MHz)
	Sequ (R)	Comb (C)		
Axcelerator (AX250 -2)	793	1,149	2	123
Proasic3 (A3P400 -2)	801	1,678	2	77
Fusion (AFS1500 -2)	801	1,678	2	72

Support

The SDR-SDRAM-CTRL core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The SDR-SDRAM-CTRL core has been verified through extensive simulation and rigorous code coverage measurements. It has also been proven in FPGA prototyping boards.

Deliverables

The SDR-SDRAM-CTRL is available as a soft core (synthesizable HDL) for ASIC technologies and as a firm core (netlist) for FPGA technologies, and includes everything required for successful implementation. The Actel version includes:

- Post Synthesis EDIF.
- Place & Route scripts.
- Simulation script, vectors and expected results.
- Sophisticated HDL Testbench.
- Comprehensive user documentation, including detailed specifications and a system integration guide.

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