

# A high-efficiency rectifier for passive UHF RFID with wide incident power range

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**Abstract:** This paper presents a rectifier for passive UHF RFID tags with high power conversion efficiency (PCE) over a wide incident power range under the influence of mismatch between tag antenna and chip, which benefits read and write sensitivities simultaneously. Fabricated with 0.13  $\mu$ m CMOS technology, the RF frontend adopting this rectifier achieves PCE higher than 25% with incident power from -19.2 dBm to -7.6 dBm. **Keywords:** power conversion efficiency (PCE), radio frequency identification (RFID), rectifier, wide power range

Classification: Integrated circuits

#### References

- [1] Quanray Electronics: Qstar-5 datasheet (2013) http://www.quanray.com/en/ home.asp.
- [2] K. Kotani, A. Sasaki and T. Ito: IEEE J. Solid-State Circuits 44 (2009) 3011.
  DOI:10.1109/JSSC.2009.2028955
- [3] E. M. Camacho-Galeano, C. Galup-Montoro and M. C. Schneider: IEEE Trans. Circuits Syst. II, Exp. Briefs 52 (2005) 61. DOI:10.1109/TCSII.2004.842059
- [4] S. Scorcioni, L. Larcher and A. Bertacchini: IEEE Microw. Compon. Lett. 23 (2013) 155. DOI:10.1109/LMWC.2013.2243376

## 1 Introduction

The power for baseband and memory of a RFID tag is largely determined by the rectifier PCE and matching efficiency (q) between tag antenna and chip for a certain operating distance. Normally writing needs more power than reading because of high voltage generation for none-volatile memory, and write sensitivity is about  $4 \sim 10 \text{ dB}$  larger than read sensitivity [1]. So high rectifier PCE and good impedance matching are required over a wide incident power range that includes read and write sensitivities. Among all the RF modules, the rectifier plays the crucial role in impedance matching.

In this paper, a novel rectifier topology is developed to work with small RF signal and to keep the input impedance relatively stable with different incident power. This leads to high read and write sensitivities at the same time.





#### 2 Rectifier analysis and design

2.1 Differential-drive rectifier



Fig. 1. A cell of the differential-drive rectifier [2].

The differential-drive rectifier shown in Fig. 1 is a typical typology for small RF signal amplitude  $(A_{RF})$  [2]. This rectifier has a cross-coupled CMOS configuration, and the gates of rectifying transistors are actively biased by a differential-mode signal.

#### 2.2 Wide incident power range

The impedance mismatching between tag antenna and chip is the main negative impact on power transfer efficiency over a wide incident power range. Based on the power transfer model, the matching efficiency (q) is described in Eq. (1),

$$q = \frac{4 \cdot R_{ant} \cdot R_{in}}{\left(R_{ant} + R_{in}\right)^2 + \left(X_{ant} + X_{in}\right)^2} \tag{1}$$

where  $R_{ant}$  ( $X_{ant}$ ) and  $R_{in}$  ( $X_{in}$ ) are the real (imaginary) part of antenna and chip impedance, respectively.

Obviously, matching efficiency is much more sensitive to the imaginary part, because it only appears in denominator and it is Q (quality factor) times larger than real part.  $X_{in}$  is determined by the equivalent parallel capacitor  $C_p$  for a certain working frequency.  $C_p$  in CMOS technology is mainly made up of  $C_{GS}$ ,  $C_{GD}$ , and  $C_{DB}$  of the rectifying transistors. Because these capacitors vary with different conduction angle ( $\theta_{on}$ ) at fixed transistor dimensions, it is important to keep  $\theta_{on}$  stable over a wide incident power range for the joint optimization of read and write sensitivities. The conduction angle of the basic differential-drive rectifier is shown in Fig. 2. The large threshold voltage ( $V_{th}$ ) of rectifying transistors leads to small  $\theta_{on}$  with low incident power and a big variation when incident power gets larger.

#### 2.3 Proposed rectifier topology

In order to decrease the deviation of  $\theta_{on}$ , a novel rectifier topology is proposed shown in Fig. 3. The rectifying transistors include MN1, MN4, MP1 and MP4. The mirror transistors (MN2, MN3, MP2 and MP4) generate DC bias voltage to adjust the turn-on voltage of the rectifying transistors. The differential RF signals are used







Fig. 2. Conduction angle of the basic differential-drive rectifier for different RF signal amplitudes.



Fig. 3. A cell of the proposed rectifier topology.

to get large conduction angle and small reverse leakage current, just like the differential-drive rectifier [2]. DC bias signals and differential RF signals are superimposed by resistors (R).

The conduction angle of the proposed rectifier is shown in Fig. 4. With the assistance of DC bias, the proposed rectifier has an "adjustable" threshold voltage. Good impedance match over a wide incident power range is achieved by small deviation of  $\theta_{on}$ . This rectifier also works efficiently with small  $A_{RF}$  (large  $\theta_{on}$ ).

#### 2.4 Cp simulation

The equivalent parallel capacitors Cp of the differential-drive rectifier cell [2] and the proposed rectifier cell are simulated as shown in Fig. 5 ( $W_p = 18$  um,  $W_n = 6$  um, L = 200 nm). The  $C_p$  deviation of the proposed rectifier is much smaller than that of the differential-drive rectifier for a certain  $A_{RF}$  variation.







Fig. 4. Conduction angle of the proposed rectifier for different RF signal amplitudes.



**Fig. 5.** (a) Equivalent parallel capacitors  $C_p$  as functions of RF signal amplitude  $A_{RF}$ , (b)  $C_p$  are normalized by the parallel capacitors with  $A_{RF} = 400$  mV, respectively.

## 2.5 Auxiliary bias circuit

The bias currents (*IBN* and *IBP*) are generated by an auxiliary circuit, which consists of two rectifiers and an automatic current generator. One rectifier made up with native NMOS transistors generates the positive power source *VDD\_BIAS*. Another rectifier composed of low threshold voltage in deep N well (DNW) generates the negative power source *VSS\_BIAS*. Native NMOS and low threshold NMOS can work with small  $A_{RF}$  because of low threshold voltage. The circuit generates the reference current automatically [3] and provides all the bias currents via current mirrors.

#### 3 Experimental results

#### 3.1 Chip fabrication

A 6-stage rectifier with the proposed topology is fabricated along with a modulator and a demodulator. A voltage regulator and storage capacitor are also included. The fabricated RF frontend is shown in Fig. 6.







Fig. 6. Micrograph of the fabricated RF frontend.

## 3.2 Equivalent model test

The equivalent model of the RF frontend as a function of incident power is shown in Fig. 7. Thus it can be seen the equivalent parallel capacitor  $C_p$  keeps relatively stable and leads to good impedance matching. The power loss from mismatching is within 10% from -22.5 dBm to -10.2 dBm (Fig. 7(c)), including the usual read and write sensitivities.



Fig. 7. (a) The equivalent series resistor Rs as a function of incident power Pin, (b) The equivalent parallel capacitor Cp as a function of incident power Pin, (c) Power loss from mismatching as a function of incident power Pin, with a custom antenna of  $17 \Omega + 35$  nH.

## 3.3 PCE test

The output DC power as a function of incident power *Pin* is shown in Fig. 8(a). Assuming that a read operation needs a power consumption of  $3 \mu$ W, the read sensitivity of the RF frontend is as high as -19.3 dBm at 915 MHz. Fig. 8(b) displays the PCE of the RF frontend as a function of incident power *Pin*. PCE under the influence of mismatching is higher than 25% with incident power from





-19.2 dBm to -7.6 dBm. The PCE of the pure rectifier is higher than the PCE of the entire RF frontend, because the demodulator dissipates some RF power.



**Fig. 8.** (a) Output DC power as a function of incident power *Pin*, (b) PCE of RF frontend as a function of incident power *Pin*.

# 3.4 Comparison

The measurement results compared with [4] are shown in Table I, as [4] is the only reported design for wide incident power range with the influence of mismatching. The proposed RF frontend has small impedance mismatching over a wide power range and a higher PCE with low incident power.

Table I. Comparison with relevant literature

|                              | [4] LMWC, 2013 | This work           |
|------------------------------|----------------|---------------------|
| Technology                   | CMOS 0.13 um   | CMOS 0.13 um        |
| Frequency                    | 868 MHz        | 915 MHz             |
| Components                   | Rectifier      | RF frontend         |
| 10% power loss from mismatch | /              | -22.5 dBm~-10.2 dBm |
| PCE with low incident power  | 14%@-20 dBm    | 23%@-20 dBm         |

## 4 Conclusion

This paper proposes a novel rectifier topology for small RF signal amplitude and wide incident power range. A RF frontend adopting this rectifier is designed and fabricated. The PCE of the RF frontend remains higher than 25% over 11.6 dB  $(-19.2 \sim -7.6 \text{ dBm})$ , proving the effectiveness of the proposed typology to widen the operation incident power range.

